NANDHA ENGINEERING COLLEGE

(An Autonomous Institution affiliated to Anna University Chennai and approved by AICTE, New Delhi)
Erode-638 052, Tamilnadu, India, Phone: 04294 – 225585

Curriculum and Syllabus
for
M.E - VLSI Design [R13]

(This Curriculum and Syllabi are applicable to Students admitted from the academic year 2013-2014 onwards)

AUGUST 2013

Approved in the First Governing body

M.E. (VLSI DESIGN)

SEMESTER I

THEORY					
Course code	**Course Title**	**L**	**T**	**P**	**C**
13AE101	Applied Mathematics for Electronics Engineers	3	1	0	4
13VL101	DSP Integrated Circuits	3	0	0	3
13AE103	Advanced Digital System Design	3	0	0	3
13VL102	VLSI Design Techniques	3	0	0	3
13VL103	Solid State Device Modelling and Simulation	3	0	0	3
E1	Elective I	3	0	0	3

PRACTICAL					
Course code	**Course Title**	**L**	**T**	**P**	**C**
13VL116	VLSI Design Lab I	0	0	4	2
	TOTAL	**18**	**1**	**4**	21

SEMESTER II

THEORY					
Course code	**Course Title**	**L**	**T**	**P**	**C**
13AE201	Analysis and Design of Analog Integrated Circuits	3	0	0	3
13VL201	CAD for VLSI Circuits	3	0	0	3
13AE202	Computer Architecture and Parallel Processing	3	0	0	3
13AE204	Embedded Systems	3	0	0	3
E2	Elective II	3	0	0	3
E3	Elective III	3	0	0	3

PRACTICAL					
Course code	**Course Title**	**L**	**T**	**P**	**C**
13VL215	VLSI Design Lab II	0	0	4	2
	TOTAL	**18**	**0**	**4**	**20**

SEMESTER III

THEORY					
Course code	**Course Title**	**L**	**T**	**P**	**C**
E4	Elective IV	3	0	0	3
E5	Elective V	3	0	0	3
E6	Elective VI	3	0	0	3

PRACTICAL					
Course code	**Course Title**	**L**	**T**	**P**	**C**
13VL331	Project Work (Phase I)	0	0	12	6
	TOTAL	**9**	**0**	**12**	15

SEMESTER IV

PRACTICAL					
Course code	**Course Title**	**L**	**T**	**P**	**C**
13VL431	Project Work (Phase II)	0	0	24	12
	TOTAL	**0**	**0**	**24**	**20**

M.E. (VLSI DESIGN)

I TO VI SEMESTERS (PART TIME) CURRICULUM AND SYLLABUS

SEMESTER I

THEORY					
Course code	**Course Title**	**L**	**T**	**P**	**C**
13AE101	Applied Mathematics for Electronics Engineers	3	1	0	4
13AE103	Advanced Digital System Design	3	0	0	3
13VL 102	VLSI Design Techniques	3	0	0	3

PRACTICAL					
Course code	**Course Title**	**L**	**T**	**P**	**C**
13VL116	VLSI Design Lab I	0	0	4	2
	TOTAL	**9**	**1**	**4**	12

SEMESTER II

THEORY					
Course code	**Course Title**	**L**	**T**	**P**	**C**
13AE201	Analysis and Design of Analog Integrated Circuits	3	0	0	3
13VL201	CAD for VLSI Circuits	3	0	0	3
13AE204	Embedded Systems	3	0	0	3

PRACTICAL					
Course code	**Course Title**	**L**	**T**	**P**	**C**
13VL215	VLSI Design Lab II	0	0	4	2
	TOTAL	**9**	**0**	**4**	**11**

SEMESTER III

THEORY					
Course code	**Course Title**	**L**	**T**	**P**	**C**
13VL101	DSP Integrated Circuits	3	0	0	3
13VL103	Solid State Device Modeling and Stimulation	3	0	0	3
E1	Elective I	3	0	0	3
	TOTAL	**9**	**0**	**0**	**9**

SEMESTER IV

THEORY					
Course code	**Course Title**	**L**	**T**	**P**	**C**
13AE202	Computer Architecture and Parallel Processing	3	0	0	3
E2	Elective II	3	0	0	3
E3	Elective III	3	0	0	3
	TOTAL	**9**	**0**	**0**	**9**

SEMESTER V

THEORY					
Course code	**Course Title**	**L**	**T**	**P**	**C**
E4	Elective IV	3	0	0	3
E5	Elective V	3	0	0	3
E6	Elective VI	3	0	0	3

PRACTICAL					
Course code	**Course Title**	**L**	**T**	**P**	**C**
13VL331	Project Work(phase I)	0	0	12	6
	TOTAL	**9**	**0**	**12**	**6**

SEMESTER VI

PRACTICAL					
Course code	**Course Title**	**L**	**T**	**P**	**C**
13VL431	Project Work (phase II)	0	0	24	12
	TOTAL	**0**	**0**	**24**	**12**

LIST OF ELECTIVES

M.E VLSI DESIGN

ELECTIVES					
Course code	**Course Title**	**L**	**T**	**P**	**C**
13VLX01	Testing of VLSI Circuits	3	0	0	3
13VLX02	Low Power VLSI Design	3	0	0	3
13VLX03	VLSI Signal Processing	3	0	0	3
13VLX04	Analog VLSI Design	3	0	0	3
13VLX05	Design of Semiconductor Memories	3	0	0	3
13VLX06	VLSI Technology	3	0	0	3
13VLX07	Physical Design of VLSI Circuits	3	0	0	3
13VLX08	Genetic Algorithms and their Applications	3	0	0	3
13AE104	Advanced Microprocessors and Microcontrollers	3	0	0	3
13AEX02	Neural Networks and Its Applications	3	0	0	3
13VLX09	ASIC Design	3	0	0	3
13AEX05	Electromagnetic Interference and Compatibility in System Design	3	0	0	3
13VLX10	Digital Speech Signal Processing	3	0	0	3
13VLX11	DSP Processor Architecture and programming	3	0	0	3
13VLX12	Introduction to MEMS System Design	3	0	0	3

13AE101 APPLIED MATHEMATICS FOR ELECTRONIC ENGINEERS

L	T	P	C
3	1	0	4

OBJECTIVE:

The course aims at imparting the knowledge of propositions, decompositions and optimality. The course aims at providing necessary mathematical support and confidence to tackle real life problems.

LEARNING OUTCOME:

At the end of the course the students should be able

- To develop efficient algorithms for solving dynamic programming problems, to acquire skills in handling situation involving random variable.
- To learn the basics and gained the skill for specialized studies and research.
- T o exposed the basic characteristic features of a queueing system and acquire skills in analysing queueing models.
- To understand the basic principles of fuzzy logic.

UNIT I:FUZZY LOGIC **(9 + 3)**

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers..

UNIT II:MATRIX THEORY **(9 + 3)**

Some important matrix factorizations – The Cholesky decomposition – QR factorization – Least squares method – Singular value decomposition – Toeplitz matrices and some applications.

UNIT III:ONE DIMENSIONAL RANDOM VARIABLES **(9 + 3)**

Random variables – Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random variable.

UNIT IV:DYNAMIC PROGRAMMING **(9 +3)**

Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.

UNIT V:QUEUEING MODELS **(9 + 3)**

Poisson Process – Markovian queues – Single and Multi-server Models – Little's formula – Machine Interference Model – Steady State analysis – Self Service queue.

TUTORIAL : 15
TOTAL : 60 Hours

REFERENCES:

1 .George J. Klir and Yuan, B., Fuzzy sets and fuzzy logic, Theory and applications, Prentice Hall of India Pvt. Ltd., 1997.

2. Moon, T.K., Sterling, W.c., Mathematical methods and algorithms for signal processing, Pearson Education, 2000.

3. Richard Johnson, miler & Freund. , Probability and Statistics for Engineers, 7th Ed., Prentice – Hall of India, Private Ltd., New delhi(2007).

4. Taha, H.A., Operations Research, An introduction, 7th Ed., Pearson education editions, Asia, New Delhi, 2002.

5. Donald Gross and carl M. Harris, Fundamentals of Queueing theory, 2nd Ed., John Wiley and Sons, New York(1985).

13VL101 DSP INTEGRATED CIRCUITS

L	T	P	C
3	0	0	3

OBJECTIVE:

To study the detail about different architecture and design of DSP integrated circuits.

LEARNING OUTCOME:

At the end of the course the students would

- Have learnt the basics of DSP integrated circuits and VLSI circuit technologies
- Have gained a well founded knowledge of DFT and FFT.
- Have obtained FIR filters and Word length effects.
- To the detail structure of different architecture

UNIT I:DSP INTEGARTED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES (9)

Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOStechnologies.

UNIT II:DIGITAL SIGNAL PROCESSING (9)

Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal-processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.

UNIT III:DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS (9)

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems,Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT IV:DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES (9)

DSP system architectures, Standard DSP architecture, Ideal DSP architectures,Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit –serial PEs.

UNIT V:ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN (9)

Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size,Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor,DCT processor and Interpolator as case studies. Cordic algorithm.

TOTAL : 45 Hours

REFERENCES:

1. Lars Wanhammer, "DSP Integrated Circuits", 1999 Academic press, New York.
2. A.V.Oppenheim et.al, "Discrete-time Signal Processing", Pearson Education, 2000.
3. Emmanuel C. Ifeachor, Barrie W. Jervis, "Digital signal processing –A practical approach", 2nd Ed., Pearson Education, Asia.
4. Keshab K.Parhi,"VLSI Digital Signal Processing Systems design and Implementation", John Wiley & Sons, 1999.

13AE103 ADVANCED DIGITAL SYSTEM DESIGN

L	T	P	C
3	0	0	3

OBJECTIVE:

The course will provide knowledge about Synchronous and Asynchronous sequential machines with various techniques for testing the fault occurring in digital systems.

LEARNING OUTCOME:

At the end of the course the students would

- Analysis and Design of Synchronous and Asynchronous sequential machines
- Have ability to draw a ASM chart for digital designs
- Have idea about different faults in digital circuits and methods of detection and diagnosing
- Know about architecture of PLD's, FPGA's and designing of FSM
- Get programming knowledge to design a digital system using VHDL

UNIT I:SEQUENTIAL CIRCUIT DESIGN (9)

Analysis of clocked synchronous sequential circuits and modeling-State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits-design of iterative circuits-ASM chart and realization using ASM

UNIT II:ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN (9)

Analysis of asynchronous sequential circuit –flow table reduction-races-state assignment-transition table and problems in transition table-design of asynchronous sequential circuit-Static, dynamic and essential hazards –data synchronizers – mixed operating mode asynchronous circuits –designing vending machine controller

UNIT III:FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS (9)

Fault table method-path sensitization method –Boolean difference method-D algorithm -Tolerance techniques –The compact algorithm –Fault in PLA –Test generation-DFT schemes –Built in self test

UNIT IV:SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES (9)

Programming logic device families –Designing a synchronous sequential circuit using PLA/PAL –Realization of finite state machine using PLD –FPGA –Xilinx FPGA-Xilinx 4000

UNIT V:SYSTEM DESIGN USING VHDL (9)

VHDL operators –Arrays –concurrent and sequential statements –packages-Data flow –Behavioral –structural modeling –compilation and simulation of VHDL code –Test bench -Realization of combinational and sequential circuits using HDL –Registers –counters –sequential machine –serial adder –Multiplier-Divider –Design of simple microprocessor

Total = 45 Hours

REFERENCES:

1. Charles H.Roth Jr "Fundamentals of Logic Design" Thomson Learning 2004
2. Nripendra N Biswas "Logic Design Theory" Prentice Hall of India, 2001
3. Parag K.Lala "Fault Tolerant and Fault Testable Hardware Design" B S Publications, 2002
4. Parag K.Lala "Digital system Design using PLD" B S Publications, 2003
5. Charles H Roth Jr."Digital System Design using VHDL" Thomson learning, 2004
6. Douglas L.Perry "VHDL programming by Example" Tata McGraw.Hill -2006

13VL102 VLSI DESIGN TECHNIQUES

L	T	P	C
3	0	0	3

OBJECTIVE:

The course aims to develop the skills of the students in the areas of the CMOS VLSI design concepts as well as concerns related to combinational , sequential, Interconnect, and datapath systems are extremely important for today's digital designers.

LEARNING OUTCOME:

At the end of the course the students would

- To introduce the fundamental principles of VLSI circuit design.
- To examine the basic building blocks of large-scale digital integrated circuits
- To study the concepts on different levels of power estimation and optimization techniques
- implementation of special purpose structures for complex digital systems

UNIT I:MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY (9)

NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations-Second order effects. MOS models and small signal AC characteristics. Basic CMOS technology.

UNIT II:INVERTERS AND LOGIC GATES (9)

NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT III : CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION (9)

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing .Scaling.

UNIT IV:VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN (9)

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers.Physical design – Delay modelling ,cross talk, floor planning, power distribution. Clock distribution. Basics of CMOS testing.

UNIT V:VERILOG HARDWARE DESCRIPTION LANGUAGE (9)

Overview of digital design with Verilog HDL, hierarchical modelling concepts, modules and port definitions, gate level modelling, data flow modelling, behavioral modelling, task & functions, Test Bench.

TOTAL: 45 Hours

REFRENCES:

1. Neil H.E.Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education Asia, 2nd Ed.,2000
2. John.P.Uymura"Introduction to VLSI Circuits and Systems", John Wiley & Sons, Inc 2002
3. Samir Palnitkar, "Verilog HDL", Pearson Education, 2nd Ed., 2004.
4. Eugene D.Fabricius, Introduction to VLSI Design McGraw Hill International Editions, 1990.
5. J.Bhasker, B.S.Publications, "A Verilog HDL Primer", 2nd Ed., 2001.
6. Pucknell, "Basic VLSI Design", Prentice Hall of India Publication, 1995.

13VL103 SOLID STATE DEVICE MODELING AND SIMULATION

L	T	P	C
3	0	0	3

OBJECTIVE:

The **c**ourse aims to develop the skills of the students in MOSFET/CMOS technology needed to meet the requirements on speed, complexity, circuit density and power consumption.

LEARNING OUTCOME:

At the end of the course the students would

- Have learnt the basics of MOS physics and modeling of MOS structures, MOSFETS, resistance, capacitance and inductance.
- Have obtained noise modeling and modeling for accurate distortion analysis in analog CMOS circuits.
- Have learnt the basics of BSIM modeling and other MOSFET models .
- Have grasped the concept of non-quasi-static modeling and noise model temperature effects.

UNIT I:MOSFET DEVICE PHYSICS (9)

MOSFET capacitor, Basic operation, Basic modeling, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors.

UNIT II:NOISE MODELING (9)

Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, model for accurate distortion analysis, nonlinearities in CMOS devices and modeling, calculation of distortion in analog CMOS circuits

UNIT III:BSIM4 MOSFET MODELING (9)

Gate dielectric model, Enhanced model for effective DC and AC channel length and width, Threshold voltage model, Channel charge model, mobility model, Source/drain resistance model, I-V model, gate tunneling current model, substrate current models, Capacitance models, High speed model, RF model, noise model, junction diode models, Layout-dependent parasitic model.

UNIT IV:OTHER MOSFET MODELS (9)

The EKV model, model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, Non- quasi-static modeling, noise model temperature effects, MOS model 9, MOSAI model.

UNIT V:MODELLING OF PROCESS VARIATION AND QUALITY ASSURANCE (9)

Influence of process variation, modeling of device mismatch for Analog/RF Applications, Benchmark circuits for quality assurance, Automation of the tests

TOTAL: 45 Hours

REFERENCES:

1. Trond Ytterdal, Yuhua Cheng and Tor A. FjeldlyWayne Wolf, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd.

2. Philip E. Allen, Douglas R.Hoberg, "CMOS Analog Circuit Design", Second Edition, Oxford Press-2002.
3. Kiat Seng Yeo, Samir S.Rofail, Wang-Ling Gob, "CMOS / BiCMOS CLSI Low Voltage Power", Personeducationlow price edition2002 4..S.M.Sze, "Semiconductor Devices – Physics and Technology", John Wiley and sons 1985.

13VL116	VLSI DESIGN LAB I	L	T	P	C
		0	0	4	2

OBJECTIVE:

The course will provide the knowledge about design of logic gates, sequential & Combinationaldigital systems with analysis using SPICE tool. It also provides design skill using MATLAB, C Language and HDL and develops idea about the implementation of designs in FPGA/CPLD & DSP Processors.

LEARNING OUTCOME:

At the end of the course the students would

- Have knowledge about sequential & Combinational digital system designs
- know about Transient and DC analysis of transistor level designs
- Have skill to design and develop digital filters using DSP processors
- Have experience of real time implementations

1. Modeling of Sequential Digital system using VHDL.
2. Modeling of Sequential Digital system using Verilog.
3. Design and Implementation of ALU using FPGA.
4. Simulation of NMOS and CMOS circuits using SPICE.
5. Modeling of MOSFET using C.
6. Implementation of FFT, Digital Filters in DSP Processor.
7. Implementation of DSP algorithms using software package.
8. Implementation of MAC Unit using FPGA.

TOTAL:60 Hours

13AE201	ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS	L	T	P	C
		3	0	0	3

OBJECTIVE:

The objective of course to provide the background and the methods for the understanding of the operation of basic analogue CMOS cells, and how to design common functions.

LEARNING OUTCOME:

At the end of the course the students would

- Get idea about Active and passive components available in CMOS and their parasitic elements of first order transistor modeling for initial manual design and the limits of applicability
- To know about Behavior and design of basic analogue circuit primitives, including quantitative treatment of matching
- CMOS Op-Amp design, from simple single ended to full differential and rail-to-rail structures
- Signal and bias handling for noise immunity in mixed signal substrate
- Switched capacitor techniques and continuous time filters
- Practical issues in voltage and current scaling A/D and D/A converters
- SoC PLL clock generation subsystems

UNIT I:MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES (9)

Depletion region of a PN junction – large signal behavior of bipolar transistors- small signalmodel of bipolar transistor- large signal behavior of MOSFET- small signal model of theMOS transistors- short channel effects in MOS transistors – weak inversion in MOS transistors- substrate current flow in MOS transistor.

UNIT II:CIRCUIT CONFIGURATION FOR LINEAR IC (9)

Current sources, Analysis of difference amplifiers with active load using BJT and FET, supply and temperature independent biasing techniques, voltage references. Output stages: Emitter follower, source follower and Push pull output stages.

UNIT III:OPERATIONAL AMPLIFIERS (9)

Analysis of operational amplifiers circuit, slew rate model and high frequency analysis, Frequency response of integrated circuits: Single stage and multistage amplifiers, Operational amplifier noise

UNIT IV:ANALOG MULTIPLIER AND PLL (9)

Analysis of four quadrant and variable trans conductance multiplier, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits: Sources of noise- Noise models of Integrated-circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise Figure and Noise Temperature

UNIT V:ANALOG DESIGN WITH MOS TECHNOLOGY (9)

MOS Current Mirrors – Simple, Cascode, Wilson and Widlar current source – CMOS Class AB output stages – Two stage MOS Operational Amplifiers, with Cascode, MOS Telescopic- Cascode Operational Amplifier – MOS Folded Cascode and MOS Active Cascode Operational Amplifiers.

TOTAL: 45 Hours

REFERENCES:

1. Gray, Meyer, Lewis, Hurst, "Analysis and design of Analog IC's", 4th Ed., Willey International, 2002.
2. Behzad Razavi, "Principles of data conversion system design", S.Chand and company ltd, 2000
3. Nandita Dasgupata, Amitava Dasgupta,"Semiconductor Devices, Modelling and Technology", Prentice Hall of India pvt. ltd, 2004.
4. Grebene, Bipolar and MOS Analog Integrated circuit design", John Wiley & sons,Inc.,2003.
5. Phillip E.Allen Douglas R. Holberg, "CMOS Analog Circuit Design", 2nd Ed.,- Oxford University Press-2003

13VL201 CAD FOR VLSI CIRCUITS

L	T	P	C
3	0	0	3

OBJECTIVE:

The course aims to develop the skills of the students to ensure that the process of building miniaturized electronic circuits, consisting mainly of semiconductor devices, called transistors, on the surface of a thin substrate of semiconductor material.

LEARNING OUTCOME:

At the end of the course the students would

- Have learnt the basics of VLSI design methodologies.
- Have gained a well founded knowledge of design rules.
- Have obtained technique in floor planning & routing.
- Have grasped the concept of simulation, modeling, and synthesis.

UNIT I:VLSI DESIGN METHODOLOGIES (9)

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods forcombinatorial optimization.

UNIT II:DESIGN RULES

(9)

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning – Circuit representation – Placement algorithms - partitioning

UNIT III:FLOOR PLANNING (9)

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV:SIMULATION (9)

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V:MODELLINGAND SYNTHESIS (9)

High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm – Assignment problem–High level transformations.

TOTAL : 45 Hours

REFERENCES:

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons,2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

13AE202 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

L	T	P	C
3	0	0	3

OBJECTIVE:

Computer Architecture and Parallel Processing aims at imparting the basic concepts of architecture and organization of computers, understanding about pipelining and parallel processing techniques, imparting knowledge about the current PC hardware

LEARNING OUTCOME:

- To understand concepts of parallel processing and design choices of implementing parallel execution within a single processor (pipeline, VLIW, and superscalar) and multiprocessor systems.
- To gain knowledge of the state of the art research topics on advanced computing systems.

UNIT I:THEORY OF PARALLELISM (9)

Parallel computer models - the state of computing, Multiprocessors and Multicomputers and Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks. Program and network properties- Conditions of parallelism.

UNIT II:PARTITIONING AND SCHEDULING (9)

Program partitioning and scheduling, Program flow mechanisms, System interconnect architectures. Principles of scalable performance – performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.

UNIT III:HARDWARE TECHNOLOGIES (9)

Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory - backplane bus systems, cache memory organisations, shared memory organisations, sequential and weak consistency models

UNIT IV:PIPELINING AND SUPERSCALAR TECHNOLOGIES (9)

Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivector and SIMD computers, Scalable, Multithreaded and data flow architectures.

UNIT V:SOFTWARE AND PARALLEL PROGRAMMING (9)

Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

TOTAL : 45 Hours

REFERENCES:

1. Kai Hwang, " Advanced Computer Architecture ", McGraw Hill International, 2001.
2. Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced Computer architecture – A design Space Approach" , Pearson Education , 2003.
3. John P.Shen, "Modern processor design . Fundamentals of super scalar processors", Tata McGraw Hill 2003.
4. Kai Hwang, "Scalable parallel computing", Tata McGraw Hill 1998.
5. William Stallings, " Computer Organization and Architecture", Macmillan Publishing Company, 1990.
6. M.J. Quinn, " Designing Efficient Algorithms for Parallel Computers", McGraw Hill International, 1994.
7. Barry, Wilkinson, Michael, Allen "Parallel Programming", Pearson Education Asia , 2002
8. Harry F. Jordan Gita Alaghband, " Fundamentals of parallel Processing", Pearson Education , 2003
9. Richard Y.Kain, " Advanced computer architecture –A systems Design Approach", PHI, 2003.

13AE204 EMBEDDED SYSTEMS

L	T	P	C
3	0	0	3

OBJECTIVE:

The course aims at providing a strong foundation for the study of Embedded system designing, development and debugging.. It provides an in-depth knowledge about hardware and software architecture and Design Methodologies

LEARNING OUTCOME:

- To study Embedded computers, their features and design with an example
- To study Embedded architectures, design & development.
- To study the networking concepts of Embedded Systems
- To study various real time Embedded algorithms
- To study various system design techniques.

UNIT I:EMBEDDED PROCESSORS (9)

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process-Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioral Description, Design Example: Model Train Controller, ARM processor- processor and memory organization.

UNIT II:EMBEDDED PROCESSOR AND COMPUTING PLATFORM (9)

Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example : Alarm Clock. Hybrid Architecture

UNIT III:NETWORKS (9)

Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network-Based design-Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller

UNIT IV:REAL-TIME CHARACTERISTICS (9)

Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off-line Versus On-line scheduling.

UNIT V:SYSTEM DESIGN TECHNIQUES (9)

Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX- System Architecture, Ink jet printer-Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.

TOTAL: 45 Hours

REFERENCES:

1. Wayne Wolf, “Computers as Components: Principles of Embedded Computing System Design”, Morgan Kaufman Publishers.
2. Jane.W.S. Liu, “Real-Time systems”, Pearson Education Asia.
3. C. M. Krishna and K. G. Shin, “Real-Time Systems” , McGraw-Hill, 1997
4. Frank Vahid and Tony Givargis, “Embedded System Design: A Unified Hardware/Software Introduction” , John Wiley & Sons.

13VL215 **VLSI DESIGN LAB II** **L T P C**
0 0 4 2

OBJECTIVE:

The course will provide the knowledge about system design, programming skill using various languages like Embedded C, Assembly level Languages and HDL. It also teach implementation of designs in FPGA/CPLD

LEARNING OUTCOME:

At the end of the course the students would

- Have knowledge about system design using different software tools
- know about efficient programming techniques
- Have idea about Embedded System development
- Have experience of real time implementations

1. Implementation of 8 Bit ALU in FPGA / CPLD.
2. Implementation of 4 Bit Sliced processor in FPGA / CPLD.
3. Implementation of Elevator controller using embedded microcontroller.
4. Implementation of Alarm clock controller using embedded microcontroller.
5. Implementation of model train controller using embedded microcontroller.
6. System design using PLL.

TOTAL:60 Hours

13VLX01	TESTING OF VLSI CIRCUITS	L	T	P	C
		3	0	0	3

OBJECTIVE:

The course will provide knowledge about basic testing and fault modeling in digital systems. Also focus on methods for generation of test for Combinational and Sequential circuits and to design the testable digital system with self test features.

LEARNING OUTCOME:

At the end of the course the students would

- Know about faults occurring in digital systems and modelling of the faults to simplifying the detection
- Have ability to generate test vectors to detect and diagnose the faults using various algorithms
- Have idea about design of testable Combinational and Sequential circuits
- Have knowledge of system level testing schemes
- Know about design of testable memory units
- Have idea about fault diagnosing using various algorithms

UNIT I:BASICS OF TESTING AND FAULT MODELLING (9)

Introduction to testing –Faults in Digital Circuits –Modelling of faults –Logical Fault Models – Fault detection –Fault Location –Fault dominance –Logic simulation –Types of simulation –Delay models –Gate Level Event –driven simulation.

UNIT II:TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS (9)

Test generation for combinational logic circuits –Testable combinational logic circuit design –Test generation for sequential circuits –design of testable sequential circuits.

UNIT III:DESIGN FOR TESTABILITY (9)

Design for Testability –Ad-hoc design –generic scan based design –classical scan based design – system level DFT approaches.

UNIT IV:SELF –TEST AND TEST ALGORITHMS (9)

Built-In self Test –test pattern generation for BIST –Circular BIST –BIST Architectures –Testable Memory Design –Test Algorithms –Test generation for Embedded RAMs.

UNIT V:FAULT DIAGNOSIS (9)

Logical Level Diagnosis –Diagnosis by UUT reduction –Fault Diagnosis for Combinational Circuits –Self-checking design –System Level Diagnosis.

TOTAL: 45 Hours

REFERENCES:

1. M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House,2002.
2. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.
3. M.L.Bushnell and V.D.Agrawal, “Essentials of Electronic Testing for Digital, Memoryand Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
4. A.L.Crouch, “Design Test for Digital IC’s and Embedded Core Systems”, Prentice Hall International, 2002.

13VLX02 LOW POWER VLSI DESIGN

L	T	P	C
3	0	0	3

OBJECTIVE:

The course aims to develop the skills of the students in the areas of Testing low power very large scale integrated (VLSI) circuits become an area of concern due to yield and reliability problems.

LEARNING OUTCOME:

At the end of the course the students would

- Have learnt the basics of low power design and physics of power dissipation .
- Have gained a well founded knowledge of logical level and circuit level power optimization
- Have obtained advanced techniques and special techniques for reducing power consumption in memories.
- Have grasped the concept of synthesis and software design for low power.

UNIT I:POWER DISSIPATION IN CMOS (9)

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices- Basic principle of low power design.

UNIT II:POWER OPTIMIZATION (9)

Logical level power optimization – Circuit level low power design – Circuit techniques for reducing power consumption in adders and multipliers.

UNIT III:DESIGN OF LOW POWER CMOS CIRCUITS (9)

Computer Arithmetic techniques for low power systems – Reducing power consumption in memories – Low power clock, Interconnect and layout design – Advanced techniques – Special techniques

UNIT IV:POWER ESTIMATION (9)

Power estimation techniques – Logic level power estimation – Simulation power analysis – Probabilistic power analysis.

UNIT V:SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER (9)

Synthesis for low power –Behavioral level transforms- Software design for low power .

TOTAL : 45 Hours

REFERENCES:

1. K.Roy and S.C. Prasad , low power CMOS VLSI circuit design, Wiley,2000
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, designing CMOS circuits for low power, Kluwer,2002
3. J.B. Kuo and J.H Lou, Low voltage CMOS VLSI Circuits, Wiley 1999.
4. A.P.Chandrakasan and R.W. Broadersen, Low power digital CMOS design, Kluwer,1995.
5. Gary Yeap, Practical low power digital VLSI design, Kluwer,1998.
6. Abdellatif Bellaouar,Mohamed.I. Elmasry, Low power digital VLSI design,s Kluwer, 1995.
7. James B. Kuo, Shin – chia Lin, Low voltage SOI CMOS VLSI Devices and Circuits. John Wiley and sons, inc 2001.

13VLX03 VLSI SIGNAL PROCESSING

L	T	P	C
3	0	0	3

OBJECTIVE:

The course aims to develop the skills of the students to ensure that VLSI signal processing, and describes ongoing developments in the area of digital signal processing processors and architectures.

LEARNING OUTCOME:

At the end of the course the students would

- Have learnt the basics of pipelining and parallel processing concepts of FIR filters.
- Have gained a well founded knowledge of retiming and strength reduction.
- Have obtained techniques of convolution and pipelining and parallel processing of IIR filters.
- Have grasped the concept of arithmetic architectures .

UNIT I:INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS (9)

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II:RETIMING,ALGORITHMICSTRENGTHREDUCTION (9)

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rankorder filters.

UNIT III:FAST CONVOLUTION,PIPELININGANDPARALLEL PROCESSING OF IIR FILTERS (9)

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined andparallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Aheadpipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV:SCALING, ROUND-OFF NOISE, BIT-LEVEL ARITHMETIC ARCHITECTURES (9)

Scaling and round-off noise – scaling operation, round-off noise, state variabledescription of digital filters, scaling and round-off noise computation, round-off noise inpipelined IIR filters, Bit-level arithmetic architectures – parallel multipliers with signextension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serialmultipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSDmultiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V:NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING (9)

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dualrail protocol.

TOTAL : 45 Hours

REFERENCES:

1. Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004

Approved in the First Governing body

13VLX04 ANALOG VLSI DESIGN

L	T	P	C
3	0	0	3

OBJECTIVE:

The course aims to develop the skills of the students to ensure that of various masks used in the fabrication process and how the masks are used to define various features of the devices on-chip. The course will also serve as a prerequisite for specialized studies and research.

LEARNING OUTCOME:

At the end of the course the students would

- Have learnt the basics of CMOS circuit techniques and basic BICMOS circuit technique.
- Have gained a well founded knowledge of filters ,converters & sensors.
- Have obtained testability and VLSI interconnects.
- Have grasped the concept of statistical modeling and simulation .

UNIT I:BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW VOLTAGE SIGNAL PROCESSING (9)

Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOSTransistor- Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage BiCMOS Op- Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

UNIT II:BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT -MODE SIGNAL PROCESSING AND NEURAL INFORMATIONPROCESSING (9)

Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters- Practical Considerations in SI Circuits Biologically-Inspired Neural Networks-Floating - Gate, Low- Power Neural Networks -CMOS Technology and Models - Design Methodology Networks-Contrast Sensitive Silicon Retina.

UNIT III:SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/DCONVERTERS AND ANALOG INTEGRATEDSENSORS (9)

First-order and Second SC Circuits-Bilinear Transformation - Cascade Design-Switched-Capacitor Ladder Filter-Synthesis of Switched-Current Filter- Nyquist rate A/D Converters-Modulators for Over sampled A/D Conversion-First and Second Order and Multibit Sigma-Delta Modulators-Interpolative Modulators –Cascaded Architecture-Decimation Filtersmechanical,Thermal, Humidity and Magnetic Sensors-Sensor Interfaces..

UNIT IV:DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS (9)

Fault modelling and Simulation - Testability-Analysis Technique-Ad Hoc Methods andGeneral Guidelines-Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test Buses-Design for Electron -Beam Testablity-Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping Analog Circuits..

UNIT V: STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER AIDED DESIGN AND ANALOG AND MIXEDANALOG - DIGITAL LAYOUT (9)

Review of Statistical Concepts - Statistical Device Modeling- Statistical Circuit Simulation-Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout- Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.

TOTAL : 45 Hours

REFERENCES:

1. Mohammed Ismail, Terri Fiez, “Analog VLSI signal and Information Processing ", McGraw-Hill International Editons, 1994.
2. Malcom R.Haskard, Lan C.May, “Analog VLSI Design - NMOS and CMOS ", Prentice Hall, 1998.
3. Randall L Geiger, Phillip E. Allen, " Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits ", Mc Graw Hill International Company, 1990.
4. Jose E.France, Yannis Tsividis, “Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing ", Prentice Hall, 1994

13VLX05 DESIGN OF SEMICONDUCTOR MEMORIES

L	T	P	C
3	0	0	3

OBJECTIVE:

The course aims to develop the skills of the students to ensure that the modern digital systems require the capability of storing and retrieving largeamounts of information at high speeds.

LEARNING OUTCOME:

At the end of the course the students would

- Have learnt the basics of random access memory technologies
- Have gained a well founded knowledge of nonvolatile memories.
- Have obtained techniques of memorydesignfor testability and fault tolerance.
- Have grasped the concept of packaging technologies.

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UNIT I:RANDOM ACCESS MEMORY TECHNOLOGIES (9)

Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Strucutures-BiCMOS, DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application, Specific DRAMs.

UNIT II:NONVOLATILEMEMORIES (9)

Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-BipolarPROMs-CMOS PROMs-Erasable (UV) – Programmable Road-Only Memories (EPROMs)-Floating-GateEPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Arcitecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

UNIT III:MEMORY FAULT MODELING, TESTING, AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE (9)

RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing- Application Specific Memory Testing

UNIT IV:RELIABILITYAND RADIATION EFFECTS (9)

General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability- Reliability Test Structures-Reliability Screening and Qualification. RAM Fault Modeling, Electrical Testing, Psuedo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

UNIT V:PACKAGING TECHNOLOGIES (9)

Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques- Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magnetoresistive. Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-MemoryCards-High Density Memory Packaging Future Directions.

TOTAL : 45 Hours

REFERENCES:

1. Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability ",Prentice-Hall of India Private Limited, New Delhi, 1997.
2. Tegze P.Haraszti, “CMOS Memory Circuits”, Kluwer Academic publishers, 2001.
3. Betty Prince, “ Emerging Memories: Technologies and Trends”, Kluwer Academic publishers, 2002.

13VLX06	VLSI TECHNOLOGY	L	T	P	C
		3	0	0	3

OBJECTIVE:

The aim of the course is to provide students with a glimpse into the semiconductor industry that has brought about the technology revolution.

LEARNING OUTCOME:

At the end of the course the students would

- Good understanding of the various processing techniques used to fabricate integrated circuits and microstructures.
- One should understand the theory of the individual, processes, how they are characterized, both electrically and structurally, and the interrelationship of these processes when combined to fabricate integrated circuits or microstructures.

UNIT I:CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY AND OXIDATION (9)

Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.

UNIT II:LITHOGRAPHY AND RELATIVE PLASMA ETCHING (9)

Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments,

UNIT III:DEPOSITION, DIFFUSION, ION IMPLEMENTATION AND METALISATION (9)

Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Flick's one dimensional Diffusion Equation – Atomic Diffusion Mechanism – Measurement techniques - Range theory- Implant equipment. Annealing Shallow junction – High energy implantation – Physical vapour deposition – Patterning.

UNIT IV:PROCESS SIMULATION AND VLSI PROCESS INTEGRATION (9)

Ion implantation – Diffusion and oxidation – Epitaxy – Lithography – Etching and Deposition- NMOS IC Technology – CMOS IC Technology – MOS Memory IC technology - Bipolar IC Technology – IC Fabrication.

UNIT V:ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES (9)

Analytical Beams – Beams Specimen interactions - Chemical methods – Package types – banking design consideration – VLSI assembly technology – Package fabrication technology.

TOTAL : 45 Hours

REFERENCES:

1 .S.M.Sze, "VLSI Technology", Mc.Graw.Hill 2nd Ed., 2002.
2. Douglas A. Pucknell and Kamran Eshraghian, " Basic VLSI Design", Prentice Hall India 2003.
3. Amar Mukherjee, "Introduction to NMOS and CMOS VLSI System design Prentice Hall India.2000.
4. Wayne Wolf ,"Modern VLSI Design", Prentice Hall India.1998.

13VLX07 PHYSICAL DESIGN OF VLSI CIRCUITS

L	T	P	C
3	0	0	3

OBJECTIVE:

The course aims at providing a strong foundation for the study of physical design layout of VLSI circuits. It provides an in-depth knowledge about routing and circuit layouts.

LEARNING OUTCOME:

- To study about introduction of VLSI circuits.
- To study about Placement using top down approach.
- To study about Routing using top down approach.
- To learn in detail about Performance issues in circuit layouts.
- To learn single layer routing and cell generation.

UNIT I:INTRODUCTION TO VLSI TECHNOLOGY (9)

Layout Rules-Circuit abstraction Cell generation using programmable logic arraytransistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates,field programmable gate array(FPGA)-layout methodologies-Packaging-Computational Complexity-Algorithmic Paradigms

UNIT II:PLACEMENT USING TOP-DOWN APPROACH (9)

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic-Ratiocut-partition with capacity and i/o constrants.Floor planning: Rectangular dual floor planning- hierarchial approach- simulatedannealing- Floor plan sizing-Placement: Cost function- force directed method-placement by simulated annealingpartitioning placement- module placement on a resistive network – regular placementlinear placement.

UNIT III:ROUTING USING TOP DOWN APPROACH (9)

Fundamentals: Maze Running- line searching- Steiner trees Global Routing: Sequential Approaches-hierarchial approaches- multicommodity flow based techniques- Randomised Routing- One Step approach- Integer Linear Programming Detailed Routing: Channel Routing- Switch box routing. Routing in FPGA: Array based FPGA- Row based FPGAs.

UNIT IV:PERFORMANCE ISSUES IN CIRCUIT LAYOUT (9)

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees.Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- LinearProgramming Approach Timing Driving Routing: Delay Minimization- Click Skew-Problem- Buffered Clock Trees. Minimization: constrained via Minimizationunconstrained via Minimization- Other issues in minimization

UNIT V:SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION (9)

Planar subset problem(PSP)- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over The Cell (OTC) Routing-Multiple chip modules(MCM)- Programmable Logic Arrays- Transistor chaining- Wein Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction.

TOTAL: 45 Hours

REFERENCES :

1. Sarafzadeh, C.K. Wong, “An Introduction to VLSI Physical Design”, Mc Graw Hill International Edition 1995
2. Preas M. Lorenzatti, “ Physical Design and Automation of VLSI systems”, The Benjamin Cummins Publishers, 1998.

13VLX08 GENETIC ALGORITHMS AND THEIR APPLICATIONS

L	T	P	C
3	0	0	3

OBJECTIVE:

The course aims to develop the skills of the students to ensure that the used to generate useful solutions to optimization and search problems.

LEARNING OUTCOME:

At the end of the course the students would

- Have learnt the basics of genetic algorithms
- Have gained a well founded knowledge of genetic algorithms for VLSI design.
- Have obtained techniques of global routing.
- Have grasped the concept of power estimation.

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UNIT I:INTRODUCTION (**9)**

Introduction,GA Technology-Steady State Algorithm-Fitness Scaling-Inversion

UNIT II:GA FOR VLSI DESIGN (9)

GA for VLSI Design, Layout and Test automation- partitioning-automatic placement,routing technology,Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multiway Partitioning

UNIT III:HYBRID GENETIC (9)

Hybrid genetic – genetic encoding-local improvement-WDFR-Comparison of Cas- Standard cell placement-GASP algorithm-unified algorithm.

UNIT IV:GLOBAL ROUTING (**9)**

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures.

UNIT V:POWER ESTIMATION (9)

Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm.

TOTAL: 45 Hours

REFERENCES:

1. Pinaki Mazumder,E.MRudnick,"Genetic Algorithm for VLSI Design,Layout and test Automation", Prentice Hall,1998.
2. Randy L. Haupt, Sue Ellen Haupt, "Practical Genetic Algorithms" Wiley – Interscience,1977.
3. Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B.R. Vellasco, Marley Maria Bernard Vellasco "Evolution Electronics: Automatic Design of electronic Circuits and Systems Genetic Algorithms", CRC press, 1st Edition Dec 2001.
4. John R.Koza, Forrest H.Bennett III, David Andre , Morgan Kufmann, "Genetic Programming Automatic programming and Automatic Circuit Synthesis", 1st Ed., May 1999.

13AE104 ADVANCED MICROPROCESSORS AND MICROCONTROLLERS

L	T	P	C
3	0	0	3

OBJECTIVE:

The course aims at providing a strong foundation for the study of microprocessor and microcontrollers. It provides an in-depth knowledge about memory hierarchy, Paging, Segmentation and Pipelining.

LEARNING OUTCOME:

- To study basics of Microprocessor & various architecture.
- To study about Pentium Processor and its programming
- To study the ARM RISC architecture and its programming.
- To learn in detail about Motorola Microcontroller.
- To learn PIC Microcontroller and its functioning.

UNIT I:MICROPROCESSOR ARCHITECTURE (9)

Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file –Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline– pipeline hazards – instruction level parallelism – reduced instruction set –Computerprinciples – RISC versus CISC**.**

UNIT II:HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM (9)

CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit-Operating Modes –Paging – Multitasking – Exception and Interrupts – Instruction set –addressing modes – Programming the Pentium processor.

UNIT III:HIGH PERFORMANCE RISC ARCHITECTURE – ARM (9)

Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.

UNIT IV:MOTOROLA 68HC11 MICROCONTROLLERS (9)

Instruction set addressing modes – operating modes- Interrupsystem- RTC-SerialCommunication Interface – A/D Converter PWM and UART.

UNIT V:PIC MICROCONTROLLER (9)

CPU Architecture – Instruction set – interrupts- Timers- I2C Interfacing –UART- A/DConverter – PWM and introduction to C-Compilers.

TOTAL : 45 Hours

REFERENCES

1. Daniel Tabak , ‘’ Advanced Microprocessors” McGraw Hill.Inc., 1995
2. James L. Antonakos , “ The Pentium Microprocessor ‘’ Pearson Education , 1997.
3. Steve Furber , ‘’ ARM System –On –Chip architecture “Addision Wesley , 2000.
4. Gene .H.Miller .” Micro Computer Engineering ,” Pearson Education , 2003.
5. John .B.Peatman , “ Design with PIC Microcontroller , Prentice hall, 1997.
6. James L.Antonakos ,” An Introduction to the Intel family of Microprocessors ‘’ Pearson Education 1999.
7. Barry.B.Breg,” The Intel Microprocessors Architecture , Programming andInterfacing “ , PHI,2002.
8. Valvano "Embedded Microcomputer Systems" Thomson Asia PVT LTD first reprint 2001

13AEX02 NEURAL NETWORKS AND ITS APPLICATIONS

L	T	P	C
3	0	0	3

OBJECTIVE:

The course aims to develop the skills of the students in the areas to track the production losses and abnormally high maintenance cost assets, then find ways to reduce those losses or high costs.

LEARNING OUTCOME:

At the end of the course the students would

- Have learnt the basics of Safety margin and loading roughness on reliability.
- Have gained a well founded knowledge of modeling and simulation.
- Have obtained techniques and applications of electronics and software systems.
- Have grasped the concept of reliability testing and management.

UNIT I:PROBABILITY PLOTTING AND LOAD-STRENGTH INTERFERENCE (9)

Statistical distribution , statistical confidence and hypothesis testing ,probability plottingtechniques – Weibull, extreme value ,hazard, binomial data; Analysis of load – strength interference , Safety margin and loading roughness on reliability.

UNIT II:RELIABILITY PREDICTION, MODELLING AND DESIGN (9)

Statistical design of experiments and analysis of variance Taguchi method, Reliabilityprediction, Reliability modeling, Block diagram and Fault tree Analysis ,petric Nets, Statespace Analysis, Monte carlo simulation, Design analysis methods – quality functiondeployment, load strength analysis, failure modes, effects and criticality analysis.

UNIT III:ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY (9)

Reliability of electronic components, component types and failure mechanisms, Electronic systemreliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV:RELIABILITY TESTING AND ANALYSIS (9)

Test environments, testing for reliability and durability, failure reporting, Pareto analysis,Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modelling, reliability demonstration, reliability growth monitoring.

UNIT V:MANUFACTURE AND RELIABILITY MANAGEMENT (9)

Control of production variability, Acceptance sampling, Quality control and stressscreening, Production failure reporting; preventive maintenance strategy, Maintenanceschedules, Design for maintainability, Integrated reliability programmes , reliability andcosts, standard for reliability, quality and safety, specifying reliability, organization forreliability.

TOTAL: 45 Hours

REFERENCES:

1. Patrick D.T. O'Connor, David Newton and Richard Bromley, Practical Reliability Engineering, 4th Ed., John Wiley & Sons, 2002
2. David J. Klinger, Yoshinao Nakada and Maria A. Menendez, Von Nostrand Reinhold, New York, "AT & T Reliability Manual", 5th Edition, 1998.
3. Gregg K. Hobbs, "Accelerated Reliability Engineering - HALT and HASS", John Wiley & Sons, New York, 2000.
4. Lewis, "Introduction to Reliability Engineering", 2nd Ed., Wiley International,1996

13VLX09 ASIC DESIGN

L	T	P	C
3	0	0	3

OBJECTIVE:

The course aims to develop the skills of the students in the areas of Ability to evaluate complex conditions in which solving one problem creates other problems Use analytical methods to assess the cost of a decision .

LEARNING OUTCOME:

At the end of the course the students would

- Have learnt the basics of ASIC design flow and library design.
- Have gained a well founded knowledge of logical cells and i/o cells.
- Have obtained techniques of logic synthesis, simulation and testing.
- Have grasped the concept of ASIC construction, floor planning, placement and routing.

UNIT I:INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN (9)

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors – Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture .

UNIT II:PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS (9)

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT – Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III:PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY (9)

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 – Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV:LOGIC SYNTHESIS, SIMULATION AND TESTING (9)

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT V:ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTIN (9)

System partition - FPGA partitioning - partitioning methods - floor planning - placement -physical design flow –global routing - detailed routing - special routing - circuit extraction –DRC.

TOTAL : 45 Hours

REFERENCES:

1.M.J.S .Smith, "Application Specific Integrated Circuits, Addison -Wesley Longman Inc., 1997.

2.Farzad Nekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical Approach, PrenticeHall PTR, 2003.

3.Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2004.

4.R. Rajsuman, System-on-a-Chip Design and Test. Santa Clara, CA: Artech HousePublishers, 2000.

5.F. Nekoogar. Timing Verification of Application-Specific Integrated Circuits (ASICs).Prentice Hall PTR, 1999.

13AEX05 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN

L	T	P	C
3	0	0	3

OBJECTIVE:

The course aims to develop the skills of the students to ensure that equipment items or systems will not interfere with or prevent each other's correct operation through spurious emission and absorption of EMI.

LEARNING OUTCOME:

At the end of the course the students would

- Have learnt the basics of EMI /EMC concepts.
- Have gained a well founded knowledge of EMI principles.
- Have obtained techniques and applications of EMI.
- Have grasped the concept of EMI design of PCBs .

UNIT I:EMI/EMC CONCEPTS (9)

EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

UNIT II:EMI COUPLINGPRINCIPLES (9)

Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling ; Differential mode coupling ; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

UNIT III:EMI CONTROLTECHNIQUES (9)

Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

UNIT IV:EMC DESIGN OF PCBS (9)

Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

UNIT V:EMI MEASUREMENTS AND STANDARDS (9)

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

TOTAL: 45 Hours

REFERENCES:

1. V.P.Kodali, “Engineering EMC Principles, Measurements and Technologies”, IEEE Press, Newyork, 1996.
2. Henry W.Ott.,”Noise Reduction Techniques in Electronic Systems”, A Wiley InterScience Publications, John Wiley and Sons, Newyork, 1988.
3. Bemhard Keiser, “Principles of Electromagnetic Compatibility”, 3rd Ed., Artech house, Norwood, 1986.
4. C.R.Paul,”Introduction to Electromagnetic Compatibility” , John Wiley and Sons,Inc, 1992.
5. Don R.J.White Consultant Incorporate, “Handbook of EMI/EMC” , Vol I-V, 1988.

13VLX10 DIGITAL SPEECH SIGNAL PROCESSING

L	T	P	C
3	0	0	3

OBJECTIVE:

The course aims to develop the skills of the students to ensure that speech signals and the processing methods of these signals. The signals are usually processed in a digital representation, so speech processing can be regarded as a special case of digital signal processing

LEARNING OUTCOME:

At the end of the course the students would

- Have learnt the basics of speech mechanics.
- Have gained a well founded knowledge of time domain methods for speech processing.
- Have obtained techniques of linear predictive analysis of speech.
- Have grasped the concept of application of speech signal processing .

UNIT I:MECHANICS OF SPEECH (9)

Speech production mechanism – Nature of Speech signal – Discrete time modelling of Speech production – Representation of Speech signals – Classification of Speech sounds – Phones – Phonemes – Phonetic and Phonemic alphabets – Articulatory features. Music production – Auditory perception – Anatomical pathways from the ear to the perception of sound – Peripheral auditory system – Psycho acoustics

UNIT II:TIME DOMAIN METHODS FOR SPEECH PROCESSING (9)

Time domain parameters of Speech signal – Methods for extracting the parameters Energy, Average Magnitude – Zero crossing Rate – Silence Discrimination using ZCR and energy – Short Time Auto Correlation Function – Pitch period estimation using Auto Correlation Function

UNIT III:FREQUENCY DOMAIN METHOD FOR SPEECH PROCESSING (9)

Short Time Fourier analysis – Filter bank analysis – Formant extraction – Pitch Extraction – Analysis by Synthesis- Analysis synthesis systems- Phase vocoder— Channel Vocoder.

UNIT IV:HOMOMORPHIC SPEECH ANALYSIS (9)

Cepstral analysis of Speech – Formant and Pitch Estimation – Homomorphic Vocoders..

UNIT IV:LINEAR PREDICTIVE ANALYSIS OF SPEECH (10)

Formulation of Linear Prediction problem in Time Domain – Basic Principle – Autocorrelation method – Covariance method – Solution of LPC equations – Cholesky method – Durbin's Recursive algorithm – lattice formation and solutions – Comparison of different methods – Application of LPC parameters – Pitch detection using LPC parameters – Formant analysis – VELP – CELP.

UNIT V:APPLICATION OF SPEECH SIGNAL PROCESSING (10)

Algorithms: Spectral Estimation, dynamic time warping, hidden Markov model – Music analysis – Pitch Detection – Feature analysis for recognition –Automatic Speech Recognition – Feature Extraction for ASR – Deterministic sequence recognition – Statistical Sequence recognition – ASR systems – Speaker identification and verification – Voice response system – Speech Synthesis: Text to speech, voiceover IP.

TOTAL: 45 Hours

REFERENCES:

1. Ben Gold and Nelson Morgan, Speech and Audio Signal Processing, John Wiley and Sons Inc. , Singapore, 2004
2. L.R.Rabiner and R.W.Schaffer – Digital Processing of Speech signals – Prentice Hall -1978
3. Quatieri – Discrete-time Speech Signal Processing – Prentice Hall – 2001.
4. J.L.Flanagan – Speech analysis: Synthesis and Perception – 2nd Ed., – Berlin – 1972
5. I.H.Witten – – Principles of Computer Speech – Academic Press – 1982

13VLX11 DSP PROCESSOR ARCHITECTURE AND PROGRAMMING

L	T	P	C
3	0	0	3

OBJECTIVE:

The course aims to develop the skills of the students to ensure that Digital Signal Processing theory with its applications on systems using Digital Signal Processors signals.

LEARNING OUTCOME:

At the end of the course the students would

- Have learnt the basics of programmable DSPs.
- Have gained a well founded knowledge of TMS320C5X processor & TMS320C3X processor.
- Have obtained architecture of ADSP processors..
- Have grasped the concept of architecture and application of advanced processors .

UNIT I:FUNDAMENTALS OF PROGRAMMABLE DSPs (9)

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in PDSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

UNIT II:TMS320C5X PROCESSOR (9)

Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals.

UNITIII:TMS320C3XPROCESSOR (9)

Architecture – Data formats - Addressing modes – Groups of addressing modes- Instruction sets - Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals – Generating and finding the sum of series, Convolution of two sequences, Filter design

UNIT IV:ADSP PROCESSORS (9)

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

UNIT V:ADVANCED PROCESSORS (9)

Architecture of TMS320C54X: Pipe line operation, Code Composer studio – Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.

TOTAL : 45 Hours

REFERENCES:

1. B.Venkataramani and M.Bhaskar, "Digital Signal Processors – Architecture, Programming and Applications" – Tata McGraw – Hill Publishing Company Limited.New Delhi, 2003.
2. User guides Texas Instrumentation, Analog Devices, Motorola.

13VLX12 INTRODUCTION TO MEMS SYSTEM DESIGN

L	T	P	C
3	0	0	3

OBJECTIVE:

The course aims to develop the skills of the students to ensure that Micro sensors, Micro actuation, MEMS with micro actuators, Micro accelerometers and Micro fluidics.

LEARNING OUTCOME:

At the end of the course the students would

- Have learnt the basics of MEMS and microsystems.
- Have gained a well founded knowledge of mechanics for MEMS design.
- Have obtained technique in electrostatic design system issues.
- Have grasped the concept of optical and RF MEMS.

UNIT I:INTRODUCTION TO MEMS (9)

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Microaccelorometers and Micro fluidics, MEMS materials, Micro fabrication

UNIT II:MECHANICS FOR MEMS DESIGN (9)

Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics – actuators, force and response time, Fracture and thin film mechanics.

UNIT III:ELECTROSTATICDESIGN (9)

Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. bistable actuators.

UNIT IV:CIRCUIT AND SYSTEM ISSUES (9)

Electronic Interfaces, Feed back systems, Noise , Circuit and system issues, Case studies – Capacitive accelerometer, Peizo electric pressure sensor, Modelling of MEMS systems, CAD for MEMS.

UNIT V:INTRODUCTION TO OPTICAL AND RF MEMS (9)

Optical MEMS, - System design basics – Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF Memes – design basics, case study – Capacitive RF MEMS switch, performance issues.

TOTAL : 45 Hours

REFERENCES:

1. Stephen Santuria," Microsystems Design", Kluwer publishers, 2000.
2. Nadim Maluf," An introduction to Micro electro mechanical system design", Artech House, 2000
3. Mohamed Gad-el-Hak, editor," The MEMS Handbook", CRC press Baco Raton,2000.
4. Tai Ran Hsu," MEMS & Micro systems Design and Manufacture" Tata McGraw Hill, New Delhi, 2002.