

NANDHA ENGINEERING COLLEGE

(An Autonomous Institution affiliated to Anna University Chennai and approved by AICTE, New Delhi)
Erode-638 052, Tamilnadu, India, Phone: 04294 – 225585



**Curriculum and Syllabus
for
M.E. – VLSI Design [R22]
[CHOICE BASED CREDIT SYSTEM]**

(This Curriculum and Syllabi are applicable to Students admitted from the academic year (2022-2023) onwards)

AUGUST 2022

INSTITUTE VISION AND MISSION	
VISION	<ul style="list-style-type: none"> •To be an Institute of excellence providing quality Engineering, Technology and Management education to meet the ever changing needs of the society.
MISSION	<ul style="list-style-type: none"> •To provide quality education to produce ethical and competent professionals with social Responsibility •To excel in the thrust areas of Engineering, Technology and Entrepreneurship by solving real- world problems. •To create a learner centric environment and improve continually to meet the changing global needs.
M.E. – VLSI DESIGN	
VISION	<ul style="list-style-type: none"> •To foster academic excellence imparting knowledge in Electronics, Communication and allied disciplines to meet the ever growing needs of the society.
MISSION	<p>Post graduate programme in ME VLSI Design is committed:</p> <ul style="list-style-type: none"> •To impart quality education and develop an aptitude for professional career and continuous learning with ethics and social responsibility. •To provide a framework for research and innovation to meet the emerging challenges through regular interaction with industry. •To be a learner centric environment by upgrading knowledge and skills to cater the needs and challenges of the society.
PROGRAMME EDUCATIONAL OBJECTIVES (PEO)	<p>Post graduate of VLSI Design programme will be</p> <p>PEO1: Core Competency: Successful in industry by applying knowledge of VLSI Design Techniques.</p> <p>PEO2: Research, Innovation and Entrepreneurship: Able to identify, design and provide innovative solutions to solve real world social problems through research.</p> <p>PEO3: Ethics, Human values and Life-long learning: Demonstrate soft skills, professional and ethical values for a successful career through lifelong learning.</p>
PROGRAMME SPECIFIC OUTCOMES (PSO)	<p>At the end of this program, the students will be able to</p> <ul style="list-style-type: none"> •Apply a systematic approach to solve the problems in the field of VLSI Domain. •Design an ASIC and FPGA based system using modern Electronic Design Automation tools with knowledge, techniques and skills for the benefit of industry and society.

PROGRAM OUTCOMES:

At the end of a programme the students will be

a-f	GRADUATE ATTRIBUTES	PO No.	PROGRAMME OUTCOMES
a	Research aptitude	PO1	An ability to Independently carry out research / investigation and development work to solve practical problems.
b	Technical documentation	PO2	An ability to write and present a substantial technical report/document
c	Technical competence	PO3	Able to demonstrate a degree of mastery over the areas of VLSI Systems, IC fabrication, design, testing, verification and prototype development focusing on applications.
d	Engineering Design	PO4	An ability to Identify and apply modern hardware & software tools related to create innovative products/ systems to solve real world problems in VLSI domain
e	The engineer and society	PO5	Apply technical knowledge towards the development of socially relevant products
f	Environment and sustainability	PO6	Apply appropriate managerial and technical skills in the domain of VLSI design incorporating safety and sustainability to become a successful Professional / entrepreneur through lifelong learning

MAPPING OF PROGRAMME EDUCATIONAL OBJECTIVES WITH PROGRAMME OUTCOMES

A broad relation between the programme objective and the outcomes is given in the following table

PROGRAMME EDUCATIONAL OBJECTIVES	PROGRAMME OUTCOMES					
	A	B	C	D	E	F
1	3	3	3	3	3	2
2	2	3	3	2	3	3
3	3	2	1	1	2	2

MAPPING OF PROGRAM SPECIFIC OUTCOMES WITH PROGRAMME OUTCOMES

A broad relation between the Program Specific Objectives and the outcomes is given in the following table

PROGRAM SPECIFIC OUTCOMES	PROGRAMME OUTCOMES					
	A	B	C	D	E	F
1	3	3	3	3	2	2
2	3	3	2	3	3	2

Contribution 1: Reasonable 2: Significant 3: Strong

SEMESTER: I									
S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PRE-REQUISITE	CONTACT PERIODS	L	T	P	C
THEORY									
1	22VLA01	Graph Theory And Optimization Techniques	FC	NIL	4	3	1	0	4
2	22VLB01	Digital CMOS VLSI Design	PC	NIL	3	3	0	0	3
3	22VLB02	Semiconductor Devices and Modeling	PC	NIL	3	3	0	0	3
4	22VLA02	Digital System Design	FC	NIL	3	3	0	0	3
5	22VLB03	VLSI Signal Processing	PC	NIL	3	3	0	0	3
6	EI	Elective I	PE	Ref. PE	3	3	0	0	3
PRACTICAL									
7	22VLP01	VLSI Design Laboratory - I	PC	NIL	4	0	0	4	2
Mandatory Non Credit Courses									
8	AI	Audit Course	EEC	Ref. AC	2	2	0	0	0
TOTAL					25	20	1	4	21

SEMESTER: II									
S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PRE-REQUISITE	CONTACT PERIODS	L	T	P	C
THEORY									
1	22VLB04	Computer Aided Design for VLSI systems	PC	NIL	3	3	0	0	3
2	22VLB05	Analog VLSI Circuits	PC	22VLB02	3	3	0	0	3
3	22VLB06	Embedded System Design	PC	NIL	3	3	0	0	3
4	22VLB07	VLSI Testing	PC	NIL	3	3	0	0	3
5	E2	Elective II	PE / OE	Ref. PE/OE	3	3	0	0	3

6	E3	Elective III	PE	Ref. PE	3	3	0	0	3
PRACTICAL									
7	22VLP02	VLSI Design Laboratory - II	PC	22VLP01	4	0	0	4	2
8	22VLE01	Term Paper and Seminar	EEC		2	0	0	2	1
TOTAL					24	18	0	6	21

SEMESTER: III									
S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PRE-REQUISITE	CONTACT PERIODS	L	T	P	C
THEORY									
1	E4	Elective IV	PE	Ref. PE	3	3	0	0	3
2	E5	Elective V	PE	Ref. PE	3	3	0	0	3
3	E6	Elective VI	PE	Ref. PE	3	3	0	0	3
PRACTICAL									
4	22VLE02	Project Work (Phase- I)	EEC	NIL	12	0	0	12	6
TOTAL					21	9	0	12	15

SEMESTER: IV									
S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PRE-REQUISITE	CONTACT PERIODS	L	T	P	C
PRACTICAL									
1	22VLE03	Project Work (Phase- II)	EEC	22VLE02	24	0	0	24	12
TOTAL					24	0	0	24	12

(A) FC,PC, PE,OE, and EEC Courses									
(a) Foundation Courses (FC)									
S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PRE-REQUISITE	CONTACT PERIODS	L	T	P	C
1.	22VLA01	Graph Theory And Optimization Techniques	FC	NIL	4	3	1	0	4
2.	22VLA02	Digital System Design	FC	NIL	3	3	0	0	3

(b) Professional Core (PC)									
S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PRE-REQUISITE	CONTACT PERIODS	L	T	P	C
1.	22VLB01	Digital CMOS VLSI Design	PC	NIL	3	3	0	0	3
2.	22VLB02	Semiconductor Devices and Modeling	PC	NIL	3	3	0	0	3
3.	22VLB03	VLSI Signal Processing	PC	NIL	3	3	0	0	3
4.	22VLB04	Computer Aided Design for VLSI systems	PC	NIL	3	3	0	0	3
5.	22VLB05	Analog VLSI Circuits	PC	22VLB02	3	3	0	0	3
6.	22VLB06	Embedded System Design	PC	NIL	3	3	0	0	3
7.	22VLB07	VLSI Testing	PC	NIL	3	3	0	0	3
8.	22VLP01	VLSI Design Laboratory - I	PC	NIL	4	0	0	4	2
9.	22VLP02	VLSI Design Laboratory - II	PC	22VLP01	4	0	0	4	2

(c) Professional Electives (PE)									
S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PRE-REQUISITE	CONTACT PERIODS	L	T	P	C
1.	22VLX01	Advanced Wireless Sensor Networks	PE	NIL	3	3	0	0	3
2.	22VLX02	ASIC Design	PE	NIL	3	3	0	0	3
3.	22VLX03	Design Of Analog Filters And Signal Conditioning Circuits	PE	NIL	3	3	0	0	3
4.	22VLX04	DSP with VLSI Structure	PE	NIL	3	3	0	0	3

5.	22VLX05	Electromagnetic Interference and Compatibility in Electronic System Design	PE	NIL	3	3	0	0	3
6.	22VLX06	Electronics Packaging	PE	NIL	3	3	0	0	3
7.	22VLX07	Genetic Algorithms for VLSI Design	PE	NIL	3	3	0	0	3
8.	22VLX08	Low Power VLSI Design	PE	22VLB01	3	3	0	0	3
9.	22VLX09	MEMS and NEMS	PE	NIL	3	3	0	0	3
10.	22VLX10	Nano Scale Devices	PE	NIL	3	3	0	0	3
11.	22VLX11	Networks On Chip	PE	NIL	3	3	0	0	3
12.	22VLX12	Physical Design of VLSI Circuits	PE	22VLB04	3	3	0	0	3
13.	22VLX13	Reconfigurable Architectures	PE	22VLX02	3	3	0	0	3
14.	22VLX14	RFIC Design	PE	NIL	3	3	0	0	3
15.	22VLX15	Power Management and Clock Distribution Circuits	PE	NIL	3	3	0	0	3
16.	22VLX16	System Verilog	PE	NIL	3	3	0	0	3
17.	22VLX17	System On Chip	PE	NIL	3	3	0	0	3
18.	22VLX18	VLSI for IOT Systems	PE	NIL	3	3	0	0	3
19.	22VLX19	Soft Computing and Optimization Techniques	PE	NIL	3	3	0	0	3
20.	22VLX20	Hardware and Software Co-Design for FPGA	PE	NIL	3	3	0	0	3
21.	22VLX21	VLSI for Wireless Communication	PE	NIL	3	3	0	0	3
22.	22VLX22	Signal Integrity for High Speed Design	PE	NIL	3	3	0	0	3
23.	22VLX23	Digital Image and Video Processing	PE	NIL	3	3	0	0	3

(d) Open Elective Courses (OE)									
S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PRE-REQUISITE	CONTACT PERIODS	L	T	P	C
1.	22BAZ01	Research Methodology and IPR	OE	NIL	3	3	0	0	3
2.	22CPZ01	Machine Vision	OE	NIL	3	3	0	0	3

(e) Employability Enhancement Courses (EEC)									
S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PRE-REQUISITE	CONTACT PERIODS	L	T	P	C
1.	Ref. AC	Audit Course	EEC	NIL	2	2	0	0	0
2.	22VLE01	Term Paper and Seminar	EEC	NIL	2	0	0	2	1
3.	22VLE02	Project Work(Phase - I)	EEC	NIL	12	0	0	12	6
4.	22VLE03	Project Work (Phase - II)	EEC	22VLE02	24	0	0	24	12

(f) Audit Courses (AC)									
S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PRE-REQUISITE	CONTACT PERIODS	L	T	P	C
1.	22PGA01	English for Research Paper Writing	EEC	NIL	2	2	0	0	0
2.	22PGA02	Disaster Management	EEC	NIL	2	2	0	0	0
3.	22PGA03	Constitution of India	EEC	NIL	2	2	0	0	0

SUMMARY

SL. No.	SUBJECT AREA	CREDITS AS PER SEMESTER				CREDITS TOTAL
		I	II	III	IV	
1	FC	7	0	0	0	7
2	PC	11	14	0	0	25
3	PE	3	6	6	0	15
4	OE	0	0	3	0	3
5	EEC	0	1	6	12	19
TOTAL CREDITS		21	21	15	12	69

C. N. Ma

22VLA01 GRAPH THEORY AND OPTIMIZATION TECHNIQUES					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To introduce graph as mathematical model to solve connectivity related problems.		1.1	The students will be able to apply graph ideas is solving connectivity related problems.	
2.0	To introduce fundamental graph algorithms.		2.1	The students will be able to apply fundamental graph algorithms to solve certain optimization problems.	
3.0	To familiarize the students with the formulation and construction of a mathematical model for a linear programming problem in a real life situation.		3.1	The students will be able to formulate and construct mathematical models for linear programming problems and solve the transportation and assignment problems.	
4.0	To provide knowledge and training using non-linear programming under limited resources for engineering and business problems.		4.1	The students will be able to model various real life situations as optimization problems and effect their solution through Non-linear programming.	
5.0	To understand the applications of simulation modeling in engineering problems.		5.1	The students will be able to apply simulation modeling techniques to problems drawn from industry management and other engineering fields.	

UNIT I - GRAPHS	(9)
Graphs and graph models – Graph terminology and special types of graphs – Matrix representation of graphs and graph isomorphism – Connectivity – Euler and Hamilton paths.	
UNIT II - GRAPH ALGORITHM	(9)
Graph Algorithms – Directed graphs – Some basic algorithms – Shortest path algorithms – Depth – First search on a graph – Theoretic algorithms – Performance of graph theoretic algorithms – Graph theoretic computer languages.	
UNIT III - LINEAR PROGRAMMING	(9)
Formulation – Graphical solution – Simplex method – Two-phase method – Transportation and Assignment Models.	

UNIT IV - NON-LINEAR PROGRAMMING	(9)
Constrained Problems – Equality constraints – Lagrangean Method – Inequality constraints –Karush – Kuhn-Tucker (KKT) conditions – Quadratic Programming.	
UNIT V - SIMULATION MODELLING	(9)
Monte Carlo Simulation - Types of Simulation -Elements of Discrete Event Simulation – Generation of Random Numbers – Applications to Queuing systems	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1.Taha H.A, “Operation Research: An Introduction”, Ninth Edition, Pearson Education, NewDelhi, 2010 2.Gupta P. K, and Hira D.S., “Operation Research”, Revise Edition, S. Chand and Company Ltd., 2012. 3.Sharma J.K., “Operation Research”, 3rd Edition, Macmillan Publishers India Ltd., 2009. 4.Douglas B. West, “Introduction to Graph Theory”, Pearson Education, New Delhi, 2015. 5.Balakrishna R., Ranganathan. K., “A text book of Graph Theory”, Springer Science and Business Media, New Delhi, 2012 6.Narasingh Deo, “Graph Theory with Applications to Engineering and Computer Science”, Prentice Hall India, 1997.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	1	2	3	4	5	6	1	2
2	3	-	1	2	3	-	2	-
3	3	-	1	2	3	-	2	-
4	2	-	2	1	2	-	1	-
5	2	-	2	1	2	-	1	-
CO	3	-	2	1	1	-	1	-

C.N. Ma...

22VLB01 DIGITAL CMOS VLSI DESIGN					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives		Course Outcomes			
1.0	To enable the student to understand fabrication process of CMOS technology and its layout design rules.	1.1	The Students will be able to a Learn CMOS design rules and fabrication process.		
2.0	To make students to understand the concepts of MOS transistors operations and their models	2.1	The Students will be able to aware about the trends in MOS transistor theory and its operation		
3.0	To introduce the principles and design methodology in static and dynamic CMOS design.	3.1	The Students will be able to design Combinational circuits.		
4.0	To introduce the principles and design methodology in sequential MOS logic circuits.	4.1	The Students will be able to design sequential circuits at the transistor level and compare the tradeoffs of sequencing elements including registers and latches.		
5.0	To make the students to understand the concepts of arithmetic components and system level physical design	5.1	The Students will be examine the physical design process and analyze Adders, Multipliers and Shifters		

UNIT I - FABRICATION TECHNOLOGIES	(9)
VLSI Manufacturing Process Steps - Crystal Growth - Wafer cleaning – Oxidation - Thermal Diffusion - Ion Implantation – Lithography –Epitaxy – Metallization -Dry and Wet etching and Packaging – P -Well process, N -Well process, twin -tub process	
UNIT II – MOS TRANSISTOR THEORY	(9)
NMOS and PMOS transistors, CMOS logic, MOS transistor theory –Introduction, Enhancement mode transistor action, Ideal I-V characteristics, DC transfer characteristics, Threshold voltage-Body effect-Design equations-Second order effects. Detailed MOS gate capacitance model – Stick Diagram -and Layout Diagram and Layout Design Rules.	
UNIT III - STATIC & DYNAMIC CMOS DESIGN	(9)
CMOS Static & Complementary logic-CMOS Transmission Gates-Pass Transistor Circuit-Synchronous Dynamic Circuit-Dynamic CMOS Circuit Techniques-High performance CMOS Circuits.	

UNIT IV - SEQUENTIAL MOS LOGIC CIRCUITS	(9)
Static latches and registers, dynamic latches and registers, timing issues, pipelines, clocking strategies, nonbistable sequential circuits.	
UNIT V - VLSI SYSTEM COMPONENTS AND SYSTEM LEVEL PHYSICAL DESIGN	(9)
Arithmetic circuits–Adders, Multipliers and Shifters - Physical design –Delay modeling, cross talk, floor planning, power distribution. Clock distribution. Basics of CMOS testing.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<p>1.Neil H.E. “Weste and Kamran Eshraghian, Principles of CMOS VLSI Design”, Pearson Education ASIA, 3rd edition, 2007.</p> <p>2.Jan M. Rabaey, AnanthaChandrakasan, Borivoje Nikolic, “Digital Integrated Circuits: A Design Perspective”, PHI, 2nd Edition, 2016.</p> <p>3.Sung-Mokang, Yusuf Leblebici, Chulwoo Kim “CMOS Digital Integrated Circuits Analysis and Design”, McGraw Hill, 4th Edition, 2016.</p> <p>4.S.M.Sze, “VLSI Technology”, Mc.Graw.Hill 2nd Edition. 2002.</p>

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3		3	2	1		3	1
2	3	1	2	1	1		2	1
3	2	1	2	3	3	1	1	3
4	2	1	2	3	3	1	1	3
5	1	1	3	2	1	1	2	3
CO (W.A)	2	1	2	2	2	1	2	2

C.N.M.

22VLB02 SEMICONDUCTOR DEVICES AND MODELING					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives		Course Outcomes			
1.0	To Learn the basics of MOS capacitors.	1.1	The students will be able to know about the basics of MOSFET Operation and Modeling.		
2.0	To acquire sound knowledge in MOSFET Fabrication.	2.1	The students will be analyze the various characteristics of Small-signal Modeling.		
3.0	To understand the concept of BSIM4 MOSFET.	3.1	The students will be understand the Gate Dielectric Model.		
4.0	To study the concept of EKV model.	4.1	The students will be able to know about the characteristics of Non-quasi-static Modeling.		
5.0	To study the concept of Quality Assurance of MOSFET.	5.1	The students will be applying the Device Mismatch for Analog/RF Applications.		

UNIT I - MOSFET DEVICE	(9)
MOS Capacitor, Interface charge, Threshold Voltage, MOS Capacitance, MOS Charge Control Model, Basic MOSFET Operation and Modeling, Advanced MOSFET Modeling.	
UNIT II -MOSFET FABRICATION AND RF MODELING	(9)
Typical Planar Digital CMOS Process Flow, RF CMOS Technology, Equivalent Circuit Representation of MOS Transistors, High-frequency Behavior of MOS Transistors and AC Small-signal Modeling, Model Parameter Extraction, NQS Model for RF Applications.	
UNIT III-BSIM4 MOSFET MODEL	(9)
Gate Dielectric Model, Enhanced Models for Effective DC and AC Channel Length and Width, Threshold Voltage Model, Channel Charge Model, Mobility Model, Source/Drain Resistance Model, I-V Model, Gate Tunneling Current Model, Substrate Current Models, RF Model.	
UNIT IV - EKV MODEL	(9)
Model Features, Long-channel Drain Current Model, Modeling Second-order Effects of the Drain Current, SPICE Example: The Effect of Charge-sharing, Modeling of Charge Storage Effects, Non-quasi-static Modeling, the Noise Model, Temperature Effects, Version 3.0 of the EKV Model	

UNIT V-QUALITY ASSURANCE OF MOSFET MODELS	(9)
Effects and Modeling of Process Variation and Device Mismatch, Influence of Process Variation and Device Mismatch, Modeling of Device Mismatch for Analog/RF Applications, Motivation, Benchmark Circuits, Automation of the Tests	
TOTAL (L:45) :45 PERIODS	

REFERENCES:

1. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd, 2003.
2. A.B. Bhattacharyya "Compact MOSFET Models for VLSI Design", John Wiley & Sons Ltd, 2009.
3. Yuan Taur and Tak H.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 3rd Edition 2012.
4. Behzad Razavi, "Fundamentals of Microelectronics" Wiley Student Edition, 3rd Edition, 2021
5. Arora, N., "MOSFET Models for VLSI Circuit Simulation", Springer-Verlag, 1993

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	2	3			3	2	3	2
2	3		2	2	3		3	2
3	2	3		3	2		3	2
4	2	3	2	3			3	2
5	2	2		2		3	3	2
CO (W.A)	2.2	2.75	2	2.5	2.66	2.5	3	2

C. N. Ma

22VLA02 DIGITAL SYSTEM DESIGN					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To make the students able to analysis and design of Synchronous sequential machines	1.1	The students will be able to analysis and design of Synchronous sequential machines		
2.0	To make the students able to analysis and design of hazard free Asynchronous sequential machines	2.1	The students will be able to analysis and design of hazard free Asynchronous sequential machines.		
3.0	To make the students able to classify the faults, fault detection and diagnosing	3.1	The students will be able to classify the faults, fault detection and diagnosing		
4.0	To make the students able to classify and describe the PLD's and FPGA's	4.1	The students will be able to classify and describe the PLD's and FPGA's		
5.0	To make the students able to write program using Verilog code to design a digital system.	5.1	The students will be to write program using Verilog code to design a digital system.		

UNIT I - SEQUENTIAL CIRCUIT DESIGN	(9)
Analysis of clocked synchronous sequential circuits and modeling-State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits- ASM chart and System design using ASM Realization by using Multiplexer & PLA.	
UNIT II -ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN	(9)
Analysis of asynchronous sequential circuit – flow table reduction – races - state assignment transition table and problems in transition table - design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller	
UNIT III-FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS	(9)
Fault table method - path sensitization method – Boolean difference method - D algorithm - Tolerance techniques – Fault in PLA –Test generation - DFT schemes – Built in self test	

UNIT IV - SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES	(9)
Programming logic device families–Designing a synchronous sequential circuit using PLA/PAL Altera MAX 7000 –FPGA –Xilinx FPGA-Xilinx 4000.	
UNIT V-SYSTEM DESIGN USING VERILOG	(9)
Verilog operators – Arrays – concurrent and sequential statements –Data flow – Behavioral – structural modeling – Test bench - Using Sub circuits - Realization of combinational and sequential circuits – Registers – counters – sequential machine – serial adder – Multiplier-Divider- Introduction To System Verilog.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. Stephen Brown, Zvonko Vranesic, “ Fundamentals of Digital Logic with Verilog Design” , 2nd Edition Tata McGraw Hill, 2007. 2. Donald D. Givone “Digital Principles and Design” Tata McGraw Hill, 2003. 3. Floyd, Floyd Thomas L.” Digital Fundamentals “Pearson Education India, 2009. 4. J. Baskar “A System Verilog Primer” Star Galaxy Publishing, India, 2018. 5. Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications, 2002.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3		3	3		2	3	
2	3		3	3		2	3	
3	3		3		1	3	3	
4	3		3	2	2	3	2	3
5	3		3	3	3	3	3	3
CO (W.A)	3	0	3	2.75	2	2.6	2.8	3

C.N.M.

22VLB03 VLSI SIGNAL PROCESSING					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To make students to learn and understand the various VLSI architectures for digital signal processing.	1.1	The students will be able to implement the various DSP design using FPGA technology.		
2.0	To make the students to understand the reduction of critical path architecture design.	2.1	The students will be able to design arithmetic operations using critical path reduction.		
3.0	To make the students to understand the reduction of critical path architecture design.	3.1	The students will be able to design recursive IIR filters using Algorithmic strength reduction methods.		
4.0	To make the students to design various filters required for particular application.	4.1	The students will be able to design FIR filters using Pipelined Digital techniques.		
5.0	To motivate the students to study the performance parameters, viz. area, speed and power.	5.1	The students will be able study the performance parameters, viz. area, speed and power through Synchronous and asynchronous pipelining.		

UNIT I - INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS	(9)
Introduction to DSP systems – typical DSP algorithms, data flow and dependence graphs – critical path, loop bound, iteration bound, longest path matrix algorithm, pipelining and parallel processing of FIR filters, pipelining and parallel processing for low power.	
UNIT II - RETIMING, ALGORITHMIC STRENGTH REDUCTION	(9)
Retiming – definitions and properties, unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even, Merge-Sort architecture, parallel rank-order filters.	
UNIT III - FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS	(9)
Computer arithmetic techniques for low power system – reducing power consumption in combinational logic, sequential logic, memories – low power clock – advanced techniques – special techniques, adiabatic techniques – physical design, floor planning, placement and routing.	

UNIT IV - BIT-LEVEL ARITHMETIC ARCHITECTURES	(9)
Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters	
UNIT V - NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS WAVE AND ASYNCHRONOUS PIPELINING	(9)
Numerical strength reduction – sub-expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining - Bundled Data versus Dual-Rail protocol.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. Keshab K.Parhi, "VLSI Digital Signal Processing Systems, Design and Implementation", John Wiley, Indian Reprint, 2007. 2. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Arrays", Springer, Second Edition, Indian Reprint, 2007. 3. S.Y.Kuang, H.J. White house, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1995.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1			3					
2						2		
3	3							
4					2		2	
5				3			2	
CO (W.A)	3	-	3	3	2	2	2	

C.N.M.

22VLP01 VLSI DESIGN LABORATORY- I					
		L	T	P	C
		0	0	4	2
PRE REQUISITE : NIL					
Course Objectives		Course Outcomes			
1.0	To make the students to design and simulate the digital system using HDL codes	1.1	The Students will be able to design simulate the digital system using HDL codes		
2.0	To make the students to able to analysis the SPICE modeling of Logic gates	2.1	The Students will be able to able to analysis the SPICE modeling of Logic gates		
3.0	To make the student to able to implement the digital systems in FPGA hardware	3.1	The Students will be able to implement the digital systems in FPGA hardware		
4.0	To make the student to able to interface the sensor with FPGA hardware	4.1	The Students will be able to interface the sensor with FPGA hardware		
5.0	To make the student to able to interface the motors and sign boards with FPGA hardware	5.1	The Students will able to able to interface the motors and sign boards with FPGA hardware		

List of Experiments
<ol style="list-style-type: none"> 1. Modeling of Sequential Digital system using Verilog VHDL. 2. Modeling of Sequential Digital system using System Verilog. 3. Design and Implementation of ALU unit using FPGA. 4. Modeling of CMOS and NMOS Inverter and Logic gates using Tanner. 5. Modeling and analysis of MOS capacitor 6. Interfacing of Proximity sensor with FPGA to detect an object 7. Implementation of Stepper Motor control using FPGA. 8. Implementation of Traffic light control using FPGA.
TOTAL (P:60) :60 PERIODS

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3		3	3		2	3	
2	3		3	3		2	3	
3	3		3		1	3	3	
4	3		3	2	2	3	2	3
5	3		3	3	3	3	3	3
CO (W.A)	3		3	2.75	2	2.6	2.8	3

C. N. Ma

22VLB04 COMPUTER AIDED DESIGN FOR VLSI SYSTEMS					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives		Course Outcomes			
1.0	To introduce the VLSI design methodologies and design methods.	1.1	The Students will be able to use various VLSI design methodologies		
2.0	To introduce data structures and algorithms required for VLSI design.	2.1	The Students will be able to understand different data structures and algorithms required for VLSI design.		
3.0	To study algorithms for partitioning and placement	3.1	The Students will be able to develop algorithms for partitioning and placement		
4.0	To study algorithms for floor planning and routing.	4.1	The Students will be able to develop algorithms for floor planning and routing		
5.0	To study algorithms for modeling, simulation and synthesis.	5.1	The Students will be able to design algorithms for modeling, simulation and synthesis.		

UNIT I - INTRODUCTION	(9)
Introduction to VLSI Design Methodologies – VLSI Design Cycle – New Trends in VLSI Design Cycle – Physical Design Cycle – New Trends in Physical Design Cycle – Design Styles – Review of VLSI Design Automation Tools.	
UNIT II -DATA STRUCTURES AND BASIC ALGORITHMS	(9)
Introduction to Data Structures and Algorithms – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable Problems – General Purpose Methods for Combinatorial Optimization.	
UNIT III -ALGORITHMS FOR PARTITIONING AND PLACEMENT	(9)
Layout Compaction – Problem Formulation – Algorithms for Constraint Graph Compaction –Partitioning – Placement – Placement Algorithms.	
UNIT IV - ALGORITHMS FOR FLOORPLANNING AND ROUTING	(9)
Floor planning – Problem Formulation – Floor planning Algorithms – Routing – Area Routing – Global Routing – Detailed Routing.	

UNIT V -MODELLING, SIMULATION AND SYNTHESIS	(9)
Simulation – Gate Level Modeling and Simulation – Logic Synthesis and Verification – Binary Decision Diagrams – High Level Synthesis.	
TOTAL (L:45) :45 PERIODS	
REFERENCES:	
<p>1. Sabih H. Gerez, “Algorithms for VLSI Design Automation”, 2nd Edition, Wiley-India, 2017.</p> <p>2.Naveed a. Sherwani, “Algorithms for VLSI Physical Design Automation”, 3rd Edition, Springer, 2017.</p> <p>3.Charles J. Alpert, Dinesh P. Mehta and Sachin S Sapatnekar, “Handbook of Algorithms for Physical Design Automation, CRC Press, 1st Edition.</p> <p>4.N.a. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.</p>	

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	2	-	2	3	-	3	2
2	3	2	1	2	3	-	3	2
3	-	-	1	-	-	1	3	2
4	3	3	2	2	3	2	3	2
5	3	3	-	2	3	-	3	2
CO (W.A)	3	2.5	1.33	2	3	1.5	3	2

C.N. Ma

22VLB05 ANALOG VLSI CIRCUITS						
			L	T	P	C
			3	0	0	3
PRE REQUISITE : 22VLB02 SEMICONDUCTOR DEVICES AND MODELING						
Course Objectives			Course Outcomes			
1.0	To study the basis of various MOS devices modeling.	1.1	The Students can be able to design MOS single stage, multistage amplifiers.			
2.0	To understand the single stage and multi stage amplifier	2.1	The Students will be able to develop design single stage and multi stage amplifier			
3.0	To expose the students to acquire knowledge in design of single stage and multistage MOS amplifier	3.1	The Students will be able to analyze Stability of single stage & multistage amplifiers.			
4.0	To analyze the current mirrors and reference circuits	4.1	The students will be able to analyze effect of transistor mismatch in analog design			
5.0	To study about the characteristics of different design parameters in designing voltage reference and OPAMP circuits	5.1	The Students will be able to design parameters common mode and differential mode gain, frequency response of OPAMP			

UNIT I - MOSFET METRICS	(9)
Simple long channel MOSFET theory – SPICE Models – Technology trend, Need for Analog design - Sub-micron transistor theory, Short channel effects, Narrow width effect, Drain induced barrier lowering, Sub-threshold conduction, Reliability, Small signal parameters, Unity Gain Frequency, Miller’s approximation.	
UNIT II - SINGLE STAGE AND TWO STAGE AMPLIFIERS	(9)
Single Stage Amplifiers – Common source amplifier with resistive load, diode load, constant current load, Source degeneration Source follower, Input and output impedance, Common gate amplifier - Differential Amplifiers-differential and common mode response, Input swing, gain, diode load and constant current load-Basic Two Stage Amplifier, Cut-off frequency.	
UNIT III - FREQUENCY RESPONSE OF SINGLE STAGE AND TWO STAGE AMPLIFIERS	(9)
Frequency Response of Single Stage Amplifiers – Noise in Single stage Amplifiers – Stability and Frequency Compensation in Single stage Amplifiers, Frequency Response of Two Stage Amplifiers – Noise in two stage Amplifiers – Stability, gain and phase margins, Frequency Compensation in two stage Amplifiers, Effect of loading in feedback networks	

UNIT IV - CURRENT MIRRORS AND REFERENCE CIRCUITS	(9)
Cascode, Negative feedback, Wilson, Regulated cascode, Bandgap voltage reference, Constant Gm biasing, supply and temperature independent reference, curvature compensation, trimming, Effect of transistor mismatch in analog design	
UNIT V - OP AMPS	(9)
Gilbert cell and applications, Basic two stage OPAMP, two-pole system response, common mode and differential gain, Frequency response of OPAMP, CMFB circuits, slew rate, power supply rejection ratio, random offset, systematic offset, OTA and OPAMP circuits - Low voltage OPAMP	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2000 2. Philip E.Allen, "CMOS Analog Circuit Design", Oxford University Press, 2013 3. Kenneth Martin Chan Carusone, David Johns , " Analog Integrated Circuit Design", Wiley Edition 2nd Edition, January 2013 4. Paul R.Gray, "Analysis and Design of Analog Integrated Circuits", Wiley Student edition, 5th edition, 2009. 5. R.Jacob Baker, "CMOS: Circuit Design, Layout , and Simulation", Wiley Student Edition, 2009

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	2	1			1	3	2
2	3	2			2		3	2
3	3		1	3		3	3	2
4		3	2	2		3	3	2
5			3	3			3	2
CO (W>A)	3	2.3	1.7	2.6	2	2.3	3	2

C.N.M.

22VLB06 EMBEDDED SYSTEM DESIGN					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives		Course Outcomes			
1.0	To understand the design challenges in embedded systems.	1.1	The student will be able to know about various design challenges in embedded system design process.		
2.0	To program the Application Specific Instruction Set Processors.	2.1	The student will be able to understand and apply knowledge of embedded hardware development tools in system design		
3.0	To understand the bus structures and protocols.	3.1	The student will be able to realize concepts about the networking principles and different protocols in embedded devices.		
4.0	To model processes using a state – machine model.	4.1	The student will be able to apply state machine techniques and design process models.		
5.0	To design a real time embedded system.	5.1	The student will be able to design suitable embedded systems for real world applications.		

UNIT I - EMBEDDED SYSTEM OVERVIEW	(9)
Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Components, Optimizing Custom Single-Purpose Processors	
UNIT II - GENERAL AND SINGLE PURPOSE PROCESSOR	(9)
Basic Architecture, Pipelining, Superscalar and VLIW Architectures, Programmer’s View, Development Environment, Application-Specific Instruction-Set Processors (ASIPS) Microcontrollers, Timers, Counters and Watchdog Timer, UART, LCD Controllers and Analog-to- Digital Converters, Memory Concepts	
UNIT III - BUS STRUCTURES	(9)
Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus - based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM bus, Wireless Protocols – IRDA, Bluetooth, IEEE 802.11.	

UNIT IV - STATE MACHINE AND CONCURRENT PROCESS MODELS	(9)
Basic State Machine Model, Finite-State Machine with Data path Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, RTOS – System design using RTOS	
UNIT V - SYSTEM DESIGN	(9)
Burglar alarm system-Design goals -Development strategy-Software development-Relevance to more complex designs- Need for emulation -Digital echo unit-Creating echo and reverb-Design requirements-Designing the codecs -The overall system design	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. Frank Vahid and Tony Gwargie, “Embedded System Design”, John Wiley & Sons, 2009. 2. Steve Heath, “Embedded System Design”, Elsevier, 2nd Edition, 2004. 3. Bruce Powel Douglas, “Real Time UML, Second Edition: Developing Efficient Objects for Embedded Systems”, 3rd Edition 2004, Pearson Education. 4. Daniel W.Lewis, “Fundamentals of Embedded Software where C and Assembly Meet”, Pearson Education, 2004.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	1	3	2	1	1	3	1
2	3	1	2	1	1	1	2	1
3	2	1	2	3	3	1	1	3
4	2	1	2	3	3	1	1	3
5	1	1	3	2	1	1	2	3
CO (W.A)	2	1	2	2	2	1	2	2

C.N.M.

22VLB07 VLSI TESTING					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To introduce the VLSI testing.		1.1	The student will be able to know about VLSI Testing Process	
2.0	To introduce logic and fault simulation and testability measures.		2.1	The student will be able to develop Logic Simulation and Fault Simulation.	
3.0	To study the test generation for combinational and sequential circuits.		3.1	The student will be able to develop Test for Combinational and Sequential Circuits.	
4.0	To study the design for testability.		4.1	The student will be able to apply the design for Testability.	
5.0	To study the fault diagnosis.		5.1	The student will be able to Perform Fault Diagnosis.	

UNIT I - INTRODUCTION TO TESTING	(9)
Introduction – VLSI Testing Process and Test Equipment – Challenges in VLSI Testing – Test Economics and Product Quality – Fault Modeling – Relationship Among Fault Models.	
UNIT II - LOGIC & FAULT SIMULATION & TESTABILITY MEASURES	(9)
Simulation for Design Verification and Test Evaluation – Modeling Circuits for Simulation – Algorithms for True Value and Fault Simulation – Scoap Controllability and Observability	
UNIT III -TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS	(9)
.Algorithms and Representations – Redundancy Identification – Combinational ATPG Algorithms – Sequential ATPG Algorithms – Simulation Based ATPG – Genetic Algorithm Based ATPG	
UNIT IV - DESIGN FOR TESTABILITY	(9)
Design for Testability Basics – Testability Analysis - Scan Cell Designs – Scan Architecture – Built in Self-Test – Random Logic BIST – DFT for Other Test Objectives.	

UNIT V -FAULT DIAGNOSIS	(9)
Introduction and Basic Definitions – Fault Models for Diagnosis – Generation of Vectors for Diagnosis – Combinational Logic Diagnosis - Scan Chain Diagnosis – Logic BIST Diagnosis.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, “VLSI Test Principles and Architectures”, Elsevier, 2017 2. Michael L. Bushnell and Vishwani D. Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits” , Kluwer Academic Publishers, 2017. 3. Niraj K. Jha and Sandeep Gupta, “Testing of Digital Systems”, Cambridge University Press, 2017.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	1	3	2	1	1	3	1
2	3	1	2	1	1	1	2	1
3	2	1	2	3	3	1	1	3
4	2	1	2	3	3	1	1	3
5	1	1	3	2	1	1	2	3
CO (W.A)	2	1	2	2	2	1	2	2

C.N.M.

22VLP02 VLSI DESIGN LABORATORY- II					
		L	T	P	C
		0	0	4	2
PRE REQUISITE : 22VLP01 VLSI DESIGN LABORATORY- I					
Course Objectives		Course Outcomes			
1.0	To make the student to able to interface the Relay with FPGA hardware	1.1	The Students will able to able to interface the Relay with FPGA hardware		
2.0	To make the student to able to interface the LCD display with FPGA hardware	2.1	The Students will able to able to interface the LCD display with FPGA hardware		
3.0	To make the student to able to interface the buzzer with FPGA hardware	3.1	The Students will be able to interface the buzzer with FPGA hardware		
4.0	To make the student to able to analysis the Layout model of logic gates	4.1	The Students will be able to analysis the Layout model of logic gates		
5.0	To make the student to able to analysis the Layout model of latch circuit	5.1	The Students will able to able to analysis the Layout model of latch circuit		

List of Experiments
<ol style="list-style-type: none"> 1. Implementation of the Relay control system in FPGA. 2. Implementation of the LCD display interface using FPGA. 3. Implementation of Seven segment display interface using FPGA. 4. Implementation of the Buzzer control using FPGA. 5. Implementation of the DC motor control using FPGA. 6. Layout level design of CMOS Inverter & NAND Gate using T-SPICE. 7. Layout level design of D- Latch Gate T-SPICE.
TOTAL (P:60) :60 PERIODS

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3		2	3		2	3	
2	2		3	2		2	2	
3	2		2		1	3	2	1
4	2		3	2	2	3	2	2
5	2		2	2	3	3	2	2
CO (W.A)	2	0	2	2	2	2.4	2	2

C. N. Ma...

22VLE01 TERM PAPER AND SEMINAR						
			L	T	P	C
			0	0	2	1
PRE REQUISITE : NIL						
Course Objectives			Course Outcomes			
I.0	To provide exposure to the students to refer, read and review the research articles in referred journals and conference proceedings.		I.1	The student will be able to write a technical report and to enhance their presentation skills.		

METHODOLOGY	<ul style="list-style-type: none"> • Each student is allotted to a faculty of the department by the HOD. By mutual discussions, the faculty guide will assign a topic in the general / Subject area to the student. •The students have to refer the Journals and Conference proceedings can collect the published literature. •The student is expected to collect at least 20 such Research Papers published in the last 5 years. •Using OHP/PowerPoint, the student has to make presentation for 15-20 minutes followed by 10 minutes discussion. •The student has to make two presentations, one at the middle and other at the end of the semester. •The student has to write a technical Report for about 30-50 pages (Title page, one page Abstract, Review of Research paper under various subheadings, Concluding Remarks and List of References).The technical report has to be submitted to the HOD one week before the final presentation ,after the approval of the faculty guide. 																
	EXECUTION	<table border="1"> <thead> <tr> <th>Week</th> <th>Activity</th> </tr> </thead> <tbody> <tr> <td>I</td> <td>Allotment of Faculty Guide by the HoD</td> </tr> <tr> <td>II</td> <td>Finalizing the topic with the approval of Faculty Guide</td> </tr> <tr> <td>III-IV</td> <td>Collection of Technical papers</td> </tr> <tr> <td>V-VI</td> <td>Mid semester presentation</td> </tr> <tr> <td>VII-VIII</td> <td>Report writing</td> </tr> <tr> <td>IX</td> <td>Report submission</td> </tr> <tr> <td>X-XI</td> <td>Final presentation</td> </tr> </tbody> </table>	Week	Activity	I	Allotment of Faculty Guide by the HoD	II	Finalizing the topic with the approval of Faculty Guide	III-IV	Collection of Technical papers	V-VI	Mid semester presentation	VII-VIII	Report writing	IX	Report submission	X-XI
Week	Activity																
I	Allotment of Faculty Guide by the HoD																
II	Finalizing the topic with the approval of Faculty Guide																
III-IV	Collection of Technical papers																
V-VI	Mid semester presentation																
VII-VIII	Report writing																
IX	Report submission																
X-XI	Final presentation																

EVALUATION	100% by Continuous Assessment 3 Hrs/week	
	Component	Weightage
	Mid semester presentation	25%
	Final presentation (Internal)	25%
	End Semester Examination Report	30%
	Presentation	20%
	Total	100%

C. N. Ma

22VLE02 - PROJECT PHASE I						
			L	T	P	C
			0	0	12	6
PRE REQUISITE : NIL						
Course Objectives			Course Outcomes			
I.0	To identify a specific problem for the current need of the society and collecting information related to the same through detailed review of literature, the methodology to solve the identified problem and preparing project reports and to face reviews and viva-voce examination.		I.1	At the end of the course the students will have a clear idea of their area of work and they will be in a position to carry out the phase II project work in a systematic way.		

SYLLABUS:

- Student individually works on a specific topic approved by the head of the department under the guidance of a faculty member who is familiar in this area.
- The student can select any topic which is relevant to the area of VLSI Design. The topic may be executed through simulators or real time hardware.
- At the end of the semester, a detailed report on the work done should be submitted which contains clear definition of the identified problem, detailed literature review related to the area of work and methodology for carrying out the work.
- The students will be evaluated through a viva-voce examination by a panel of examiners including one external examiner.

TOTAL (P:180) : 180 PERIODS

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
I	3	3	3	3	3	3	3	3
CO(W.A)	3	3	3	3	3	3	3	3

C. v. ma

22VLE03- PROJECT PHASE II					
		L	T	P	C
		0	0	24	12
PRE REQUISITE : 22VLE02					
Course Objectives		Course Outcomes			
I.0	To solve the identified problem based on the formulated methodology.	I.1	On completion of the project work students will be in a position to take up any challenging practical problem in the field of Engineering design and find better solutions to it.		

SYLLABUS:

- Student should continue the phase - I work on the selected topic as per the formulated methodology. At the end of the semester,
- After completing the work to the satisfaction of the supervisor and review committee, a detailed report should be prepared and submitted to the head of the department.
- The students will be evaluated based on the report submitted and the viva -voce examination by a panel of examiners including one external examiner.

TOTAL (P:360) : 360 PERIODS

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
I	3	3	3	3	3	3	3	3
CO (W.A)	3	3	3	3	3	3	3	3

C.N. Ma

22VLX01 ADVANCED WIRELESS SENSOR NETWORKS					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To enable the student to understand the role of sensors and the networking of sensed data for different applications		1.1	The student will be able to design and implement simple wireless network concepts	
2.0	To expose the students to the sensor node essentials and the architectural details, the medium access and routing issues and the energy constrained operational scenario.		2.1	The student will be able to analyze and implement different network architectures	
3.0	To enable the student to understand the challenges in synchronization and localization of sensor nodes, topology management for effective and sustained communication, data management and security aspects		3.1	The student will be able to implement MAC layer and routing protocols	
4.0	To design and optimize WSN architectures for various environment.		4.1	The student will be able to deal with timing and control issues in wireless sensor networks	
5.0	To enable students to design WSN with security and low power consumption.		5.1	The student will be able to analyze and design secured wireless sensor networks	

UNIT I- OVERVIEW OF WIRELESS SENSOR NETWORKS	(9)
Challenges for wireless sensor networks-characteristics requirements-required mechanisms, difference between mobile ad-hoc and sensor networks, applications of sensor networks- case study, enabling technologies for wireless sensor networks.	
UNIT II- ARCHITECTURES	(9)
Single-node architecture - hardware components, energy consumption of sensor nodes , operating systems and execution environments, network architecture - sensor network scenarios, optimization goals and figures of merit, gateway concepts. Physical layer and transceiver design considerations.	
UNIT III- MAC AND ROUTING	(9)
MAC protocols for wireless sensor networks, IEEE 802.15.4, Zigbee, low duty cycle protocols and wakeup concepts - s-MAC , mediation device protocol, wakeup radio concepts, address and name management, assignment of MAC addresses, routing protocols- energy- efficient routing, geographic routing.	

UNIT IV- INFRASTRUCTURE ESTABLISHMENT	(9)
Topology control, clustering, time synchronization, localization and positioning, sensor tasking and control.	
UNIT V- DATA MANAGEMENT AND SECURITY	(9)
Data management in WSN, storage and indexing in sensor networks, query processing in sensor, data aggregation, directed diffusion, tiny aggregation, greedy aggregation, security in WSN, security protocols for sensor networks, secure charging and rewarding scheme, secure event and event boundary detection.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:

1. Holger Karl & Andreas Willig, "Protocols and Architectures for Wireless Sensor Networks" , John Wiley, 2005.
2. Erdal Çayirci , Chunming Rong, "Security in Wireless Ad Hoc and Sensor Networks", John Wiley and Sons, 2009.
3. Kazem Sohraby, Daniel Minoli, & Taieb Znati, "Wireless Sensor Networks-S Technology, Protocols, and Applications", John Wiley, 2007.
4. Yingshu Li, My T. Thai, Weili Wu, "Wireless Sensor Networks and Applications", Springer, 2008.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	2	1				1	
2		1	2				2	1
3	3		2	1			2	
4	2			1			1	
5	1		2				2	
CO (W.A)	2.2	0.6	1.4	0.4			1.6	1

C.N. Ma

22VLX02 ASIC DESIGN					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives		Course Outcomes			
1.0	To study about Logical Effort Technique for predicting Delay, Delay Minimization and FPGA Architectures.	1.1	The student will be able to apply Logical Effort Technique for predicting Delay, Delay Minimization and FPGA Architectures.		
2.0	To familiarize the design the different types of cells.	2.1	The student will be able to Design Logic Cells and I/O Cells.		
3.0	To learn the interconnect architecture for different types of FPGA and Programmable ASIC Design software.	3.1	The student will be able to analyze the various resources of recent FPGAs.		
4.0	To gain knowledge about floor planning, placement and Routing algorithms for optimization of length and speed.	4.1	The student will be able to use algorithms for floor planning and placement of cells and to apply routing algorithms for optimization of length and speed.		
5.0	To know about SoC Design and performance.	5.1	The student will be able to analyze SoC design and its Performance.		

UNIT I - INTRODUCTION TO ASICs, CMOS LOGIC AND ASIC LIBRARY DESIGN	(9)
Types of ASICs - Design flow -CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.	
UNIT II - PROGRAMMABLE ASICs, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS	(9)
Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.	
UNIT III - PROGRAMMABLE ASIC ARCHITECTURE	(9)
Architecture and Configuration of ARTIX / Cyclone and KINTEX Ultra Scale / STRATIX FPGA – Micro-Blaze / NIOS Based Embedded Systems – Signal Probing Techniques.	

UNIT IV - LOGIC SYNTHESIS, PLACEMENT AND ROUTING	(9)
Logic Synthesis - Floor Planning Goals and Objectives, Measurement of Delay in Floor Planning, Floor Planning Tools, I/O and Power Planning, Clock Planning, Placement Algorithms. Routing: Global Routing, Detailed Routing, Special Routing.	
UNIT V - SYSTEM-ON-CHIP DESIGN	(9)
SoC Design Flow, Platform-Based and IP Based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, High Performance Filters using Delta-Sigma Modulators. Case Studies: Digital Camera, SDRAM, High Speed Data standards.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:

1. M.J.S.Smith, " Application - Specific Integrated Circuits", Pearson, 2003.
2. Steve Kilts, "Advanced FPGA Design," Wiley Inter-Science.
3. Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, "FPGA-based Implementation of Signal Processing Systems", Wiley, 2008.
4. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.
5. Douglas J. Smith, "HDL Chip Design", Madison, AL, USA: Doone Publications, 1996.
6. Jose E. France, Yannis Tsvividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.
7. S.Pasricha and N.Dutt, "On-Chip Communication Architectures System on Chip Interconnect", Elsevier, 2008.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	-	2	1	-	-	-	1
2	3	-	2	1	-	-	3	2
3	3	-	2	2	1	1	1	2
4	3	-	3	2	1	1	3	2
5	3	-	3	2	1	1	3	2
CO(W.A)	3	-	2.4	1.6	1	1	2.5	1.8

C. N. Ma

22VLX03 DESIGN OF ANALOG FILTERS AND SIGNAL CONDITIONING CIRCUITS					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To study the basis of various CMOS circuit design.	1.1	The students can be able to design CMOS circuits.		
2.0	To understand the concepts of various analog filter architectures.	2.1	The students will be able to develop analog filter architectures.		
3.0	To expose the students to acquire knowledge in signal conditioning techniques.	3.1	The students will be able to design signal conditioning circuits.		
4.0	To understand the performance of Mixed signal IC environment.	4.1	The students will be able to develop systems with Mixed signal IC environment.		
5.0	To study about the various signal conditioning circuits.	5.1	The students will be able to apply the operational and design principles for active analog filter configurations		

UNIT I - FILTER TOPOLOGIES	(9)
The Bilinear Transfer Function - Active RC Implementation, Transconductor-C Implementation, Switched Capacitor Implementation, Biquadratic Transfer Function, Active RC implementation, Switched capacitor implementation, High Q, Q peaking and instability, Transconductor-C Implementation, the Digital Biquad.	
UNIT II - INTEGRATOR REALIZATION	(9)
Low pass Filters, Active RC Integrators – Effect of finite Op-Amp Gain Bandwidth Product, Active RC SNR, gm-C Integrators, Discrete Time Integrators.	
UNIT III - SWITCHED CAPACITOR FILTER REALIZATION	(9)
Switched capacitor Technique, Biquadratic SC Filters, SC N-path filters, Finite gain and bandwidth effects, Layout consideration, Noise in SC Filters.	
UNIT IV - SIGNAL CONDITIONING TECHNIQUES	(9)
Interference types and reduction, Signal circuit grounding, Shield grounding, Signal conditioners for capacitive sensors, Noise and Drift in Resistors, Layout Techniques.	

UNIT V - SIGNAL CONDITIONING CIRCUITS	(9)
Isolation Amplifiers, Chopper and Low Drift Amplifiers, Electrometer and Trans -impedance Amplifiers, Charge Amplifiers, Noise in Amplifiers	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. Yashavant Kanetkar, "Let us C", BPB publications, New Delhi, 3 edition, 2019. 2. PradipDey, ManasGhosh, "Fundamentals of Computing and Programming in C", 1st edition, Oxford University Press, 2018. 3. Byron S Gottfried, "Programming with C", Schaum's Outlines, 2nd edition, Tata McGraw-Hill, 2017. 4. R.G. Dromey, "How to Solve it by Computer", Pearson Education, 4th Reprint, 2018.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	2	-	2	3	-	3	2
2	3	2	1	2	3	-	3	2
3	-	-	1	-	-	1	3	2
4	3	3	2	2	3	2	3	2
5	3	3	-	2	3	-	3	2
CO (W.A)	3	2.5	1.33	2	3	1.5	3	2

C.N.M.

22VLX04 DSP STRUCTURES FOR VLSI					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives		Course Outcomes			
1.0	To understand the fundamentals of DSP	1.1	The student will be able to acquired knowledge about fundamentals of DSP processors.		
2.0	To learn various DSP structures and their implementation.	2.1	The student will be able to improve the overall performance of DSP system through various transformation and optimization techniques.		
3.0	To know designing constraints of various filters	3.1	The student will be able to understand the need of different types of instructions for DSP		
4.0	To design and optimize VLSI architectures for basic DSP algorithms	4.1	The student will be able to optimize design in terms of computation complexity and speed.		
5.0	To enable students to design VLSI system with high speed and low power.	5.1	The student will be able to understand clock based issues and design asynchronous and wave pipelined systems		

UNITI-INTRODUCTION TO DSP	(9)
Linear system theory- convolution- correlation - DFT- FFT- basic concepts in FIR filters and IIR filters- filter realizations. Representations of DSP algorithms- block diagram-SFG-DFG	
UNIT II- ITERATION BOUND, PIPELINING AND PARALLEL PROCESSING OF FIR FILTER	(9)
Data-flow graph representations- Loop bound and Iteration bound algorithms for computing iteration bound-LPM algorithm. Pipelining and parallel processing: pipelining of FIR digital filters- parallel processing, pipelining and parallel processing for low power.	
UNIT III- RETIMING, UNFOLDING AND FOLDING	(9)
Retiming: definitions, properties and problems- solving systems of inequalities. Properties of Unfolding, critical path, Unfolding and Retiming, applications of Unfolding, Folding transformation- register minimization techniques, register minimization in folded architecture- folding of multirate system	

UNIT IV- FAST CONVOLUTION	(9)
Cook-toom algorithm- modified cook-Toom algorithm. Design of fast convolution algorithm by inspection	
UNIT V- ARITHMETIC STRENGTH REDUCTION IN FILTERS	(9)
Parallel FIR filters-fast FIR algorithms-two parallel and three parallel. Parallel architectures for rank order filters -odd-even, merge-sort architecture-rank order filter architecture-parallel rank order filters-running order merge order sorter, low power rank order filter	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. K.K Parhi: "VLSI Digital Signal Processing", John-Wiley, 2nd Edition Reprint, 2008. 2. John G.Proakis, Dimitris G.Manolakis, "Digital Signal Processing", Prentice Hall of India, 1st Edition, 2009

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	2	1				1	2
2		1	2				2	
3	3		2	1			2	1
4	2		3	1			1	1
5	1		2				2	1
CO(W.A)	2.2	0.6	2	0.4			1.6	1

C.N. Ma

22VLX05 ELECTROMAGNETIC INTERFERENCE AND COMPATABILITY					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To gain broad conceptual understanding of the various aspects of electromagnetic (EM) Interference and compatibility.	1.1	The student will be able to demonstrate knowledge of the various sources of electromagnetic interference.		
2.0	To develop a theoretical understanding of electromagnetic shielding effectiveness.	2.1	The student will be able to display an understanding of the effect of how electromagnetic fields couple through apertures, and solve simple problems based on that understanding.		
3.0	To understand ways of mitigating EMI by using shielding, grounding and filtering.	3.1	The student will be able to explain the EMI mitigation techniques of shielding and grounding.		
4.0	To understand the need for standards and to appreciate measurement methods.	4.1	The student will be able to explain the need for standards and EMC measurement methods.		
5.0	To understand how EMI impacts wireless and broadband technologies.	5.1	The student will be able to discuss the impact of EMC on wireless and broadband technologies.		

UNIT I - INTRODUCTION & SOURCES OF EM INTERFERENCE	(9)
Introduction - Shielding effectiveness - Far-field sources - Near-field sources - Low-frequency, magnetic field shielding - Effects of apertures	
UNIT II - EM SHIELDING	(9)
Introduction - Shielding effectiveness - Far-field sources - Near-field sources - Low-frequency, magnetic field shielding - Effects of apertures	
UNIT III - INTERFERENCE CONTROL TECHNIQUES	(9)
Equipment screening - Cable screening - grounding - Power-line filters - Isolation - Balancing - Signal-line filters - Nonlinear protective devices.	
UNIT IV - EMC STANDARDS, MEASUREMENTS AND TESTING	(9)
Need for standards - The international framework - Human exposure limits to EM fields –EMC measurement techniques - Measurement tools - Test environments. Need for standards – The international framework - Human exposure limits to EM fields –EMC measurement techniques - Measurement tools - Test environments	

UNIT V - EMC CONSIDERATIONS IN WIRELESS AND BROADBAND TECHNOLOGIES	(9)
Efficient use of frequency spectrum - EMC, interoperability and coexistence - Specifications and alliances - Transmission of high-frequency signals over telephone and power networks – EMC and digital subscriber lines - EMC and power line telecommunications.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. Christopoulos C, “Principles and Techniques of Electromagnetic Compatibility”, CRC Press, 2nd Edition, Indian Edition, 2013. 2. Clayton R.Paul,” Introduction to Electromagnetic Compatibility”, John Wiley Publications, 2008 3. Kodali V P, “Engineering Electromagnetic Compatibility”, Wiley India, Second Edition,2010. 4. Henry W Ott, “Electromagnetic Compatibility Engineering”, John Wiley & Sons Inc, Newyork, 2009. 5. Scott Bennett W, “Control and Measurement of Unintentional Electromagnetic Radiation”, John Wiley& Sons Inc., Wiley Inter science Series, 1997.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	3	2	2	3	2	3	3
2		2	2	3	3	2	2	2
3			2	3	2	2	3	2
4	3	3	3	3	2	3	2	2
5	2	3	2	3	3		3	3
CO(W.A)	2.6	2.75	2.2	2.8	2.6	2.25	2.6	2.4

C.N. Mani

22VLX06 ELECTRONICS PACKAGING					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To study the basis of various packaging types	1.1	The Students can be able to develop an electronic system PCB or integrated circuit design specifications.		
2.0	To understand the various semiconductor packages.	2.1	The Students will be able to develop Semiconductor packages.		
3.0	To expose the students to acquire knowledge in CAD based design.	3.1	The Students will be able to select the appropriate packaging style, design procedure and solution for the same.		
4.0	To understand the concept of SMD.	4.1	The students will be able to develop SMD based applications.		
5.0	To study about the characteristics of embedded passive technology.	5.1	The Students will be able to apply embedded passive technology in electronic packaging.		

UNIT I - OVERVIEW OF ELECTRONIC SYSTEMS PACKAGING	(9)
Definition of a system and history of semiconductors, Products and levels of packaging, Packaging aspects of handheld products, Definition of PWB, Basics of Semiconductor and Process flowchart, Wafer fabrication, inspection and testing, Wafer packaging; Packaging evolution; Chip connection choices, Wire bonding, TAB and flip chip.	
UNIT II - SEMICONDUCTOR PACKAGES	(9)
Single chip packages or modules (SCM), Commonly used packages and advanced packages; Materials in packages; Thermal mismatch in packages; Multichip modules (MCM)-types; System-in-package (SIP); Packaging roadmaps; Hybrid circuits; Electrical Design considerations in systems packaging, Resistive, Capacitive and Inductive Parasitics, Layout guidelines and the Reflection problem, Interconnection.	
UNIT III - CAD FOR PRINTED WIRING BOARDS	(9)
Benefits from CAD; Introduction to DFM, DFR & DFT, Components of a CAD package and its highlights, Beginning a circuit design with schematic work and component, layout, DFM check, list and design rules; Design for Reliability, Printed Wiring Board Technologies: Board-level packaging aspects, Review of CAD output files for PCB fabrication; Photo plotting and mask generation, Process flow-chart; Vias; PWB substrates; Surface preparation, Photo resist and application methods; UV exposure and developing; Printing technologies for PWBs, PWB etching; PWB etching; Resist stripping; Screen-printing technology, through-	

hole manufacture process steps; Panel and pattern plating methods, Solder mask for PWBs; Multilayer PWBs; Introduction to, micro vias, Micro via technology and Sequential build-up technology process flow for high-density, interconnects.	
UNIT IV - SURFACE MOUNT TECHNOLOGY AND THERMAL CONSIDERATIONS	(9)
SMD benefits; Design issues; Introduction to soldering, Reflow and Wave Soldering methods to attach SMDs, Solders; Wetting of solders; Flux and its properties; Defects in wave soldering, Vapour phase soldering, BGA soldering and Desoldering/Repair; SMT failures, SMT failure library and Tin Whisker, Tin-lead and lead-free solders; Phase diagrams; Thermal profiles for reflow soldering; Lead free v Alloys, Lead-free solder considerations; Green electronics; RoHS compliance and e-waste recycling, Issues, Thermal Design considerations in systems packaging.	
UNIT V - EMBEDDED PASSIVES TECHNOLOGY	(9)
Introduction to embedded passives; Need for embedded passives; Design Library; Embedded resistor processes, Embedded capacitors; Processes for embedding capacitors; Case study examples.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
1. Rao R. Tummala, "Fundamentals of Microsystems Packaging", McGraw Hill, NY, 2001
2. William D. Brown, "Advanced Electronic Packaging", IEEE Press, 1999.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	1	2	3	4	5	6	1	4
2	3	3	2	2	3	2	3	3
3		2	2	3	3	2	2	2
4			2	3	2	2	3	2
5	3	3	3	3	2	3	2	2
CO(W.A)	2.6	2.75	2.2	2.8	2.6	2.25	2.6	2.4

C.N. Mani

22VLX07 GENETIC ALGORITHMS FOR VLSI DESIGN					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To know about analysis of Genetic algorithms and layout and test automation.	1.1	The students will be able to analysis and Design of Genetic algorithms and layout and test automation.		
2.0	To draw a Circuit partitioning by genetic algorithms.	2.1	The students will be able to draw a Circuit partitioning by genetic algorithms.		
3.0	To learn about different types of Standard cell placement on a network of workstations	3.1	The students will be able to different types of Standard cell placement on a network of workstations.		
4.0	To Know about Types of genetic algorithms and parallel algorithms for ATPG	4.1	The students will be able to have knowledge of Types of genetic algorithms and parallel algorithms for ATPG		
5.0	To have knowledge about Circuit segmentation by FPGA technology.	5.1	The students will be able to design Circuit segmentation through FPGA technology		

UNIT I - FUNDAMENTALS OF GENETIC ALGORITHM	(9)
Terminologies – Simple Genetic algorithms – steady state algorithm – Genetic operators-types of GA- Genetic algorithms vs. Conventional algorithms – GA example – GA for VLSI design, layout and test automation	
UNIT II -PARTITIONING	(9)
Problem description – Circuit partitioning by genetic algorithms – hybrid genetic algorithms for ratio-cut partitioning.	
UNIT III-PLACEMENT AND ROUTING	(9)
Placement: Standard cell placement – Macro cell placement – Standard cell placement on a network of workstations Routing: Steiner problem in graph – macro cell global routing	
UNIT IV - GENETIC ALGORITHMS IN VLSI TESTING	(9)
Problem description – test generation frame work – test generation for test applications time reduction – deterministic/genetic test generators sequences-dynamic test sequence compaction – parallel algorithms for ATPG	

UNIT V-FPGA TECHNOLOGY MAPPING and PEAK POWER ESTIMATION	(9)
FPGA technology mapping: Circuit segmentation and FPGA mapping-circuit segmentation for Pseudo-Exhaustive testing. Peak power estimation: Problem description – application of GA – Estimation of peak single cycle and n-cycle powers-peak sustainable power estimation.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. Stephen Brown, Zvonko Vranesic “ Fundamentals of Digital Logic with Verilog Design” 2nd Edition Tata McGraw Hill, 2007 2. Donald D. Givone “Digital Principles and Design” Tata McGraw Hill, 2002 3. Floyd, Floyd Thomas L.” Digital Fundamentals “Pearson Education India, 2005 4. Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications, 2002 5. Parag K.Lala “Digital system Design using PLD” B S Publications, 2003.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	2	1	1	2	3	1	1
2	2	-	-	1	1	-	2	2
3	3	1	-	3	1	2	1	3
4	2	-	1	1	1	1	1	1
5	2	2	2	2	1	2	3	2
CO (W>A)	2.4	1	0.8	1.4	1.2	1.6	1.6	1.8

C.N. Ma

22VLX08 LOW POWER VLSI DESIGN					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : 22VLB01 DIGITAL CMOS VLSI DESIGN					
Course Objectives			Course Outcomes		
1.0	Identify sources of power in an IC.	1.1	The student will be able to ability to find the power dissipation of MOS circuits.		
2.0	Identify the power reduction techniques based on technology independent and technology dependent methods.	2.1	The student will be able to design and analyze various MOS logic circuits.		
3.0	Identify suitable techniques to reduce the power dissipation.	3.1	The student will be able to apply low power techniques for low power dissipation.		
4.0	Estimate Power dissipation of various MOS logic circuits.	4.1	The student will be able to able to estimate the power dissipation of ICs.		
5.0	Develop algorithms for low power dissipation.	5.1	The student will be able to ability to develop algorithm to reduce power dissipation by software.		

UNIT I - POWER DISSIPATION IN CMOS	(9)
Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design.	
UNIT II - POWER OPTIMIZATION	(9)
Logic level power optimization – Circuit level low power design – Gate level low power design – Architecture level low power design – VLSI subsystem design of adders, multipliers, PLL, low power design.	
UNIT III - DESIGN OF LOW POWER CMOS CIRCUITS	(9)
Computer arithmetic techniques for low power system – reducing power consumption in combinational logic, sequential logic, memories – low power clock – Advanced techniques – Special techniques, Adiabatic techniques.	
UNIT IV - POWER ESTIMATION	(9)
Power Estimation techniques, circuit level, gate level, architecture level, behavioral level, – logic power estimation – Simulation power analysis – Probabilistic power analysis.	

UNIT V - SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER	(9)
Synthesis for low power – Behavioral level transform –Algorithms for low power – software design for low power.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:

1. Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2000.
2. J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley 1999.
3. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995.
4. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.
5. Abdelatif Belaouar, Mohamed.I.Elmasry, “Low power digital VLSI design”, Kluwer, 1995.
6. James B.Kulo, Shih-Chia Lin, “Low voltage SOI CMOS VLSI devices and Circuits”, John Wiley and sons, inc. 2001.
7. J.Rabaey, “Low Power Design Essentials (Integrated Circuits and Systems)”, Springer, 2009

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	-	2	2	-	-	-	1
2	2	-	2	1	-	-	1	2
3	3	-	2	2	1	-	2	1
4	3	-	2	2	1	1	3	3
5	3	-	3	2	2	1	2	3
CO (W.A)	3	-	2.4	1.6	1	1	2.5	2.4

C.N.M.

22VLX09 MEMS and NEMS					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To learn about basics of MEMS and NEMS.	1.1	The student will be able to Interpret the fundamentals of MEMS and NEMS.		
2.0	To present different ways MEMS fabrication technologies.	2.1	The students will be able to understand Micro system fabrication processes and Micro system packaging.		
3.0	To provide idea about the design concepts of micro sensors.	3.1	The students will be able to deal with different types of micro sensors		
4.0	To provide idea about the design concepts of micro sensors.	4.1	The students will be able to deal with different types of micro actuators.		
5.0	It deals with the idea of nano devices.	5.1	The students will be familiarized with the concepts of nano devices.		

UNIT I - INTRODUCTION TO MEMS AND NEMS	(9)
Introduction to Design of MEMS and NEMS, Overview of Nano and Micro electromechanical Systems, Applications of Micro and Nano electromechanical systems, Materials for MEMS and NEMS: Silicon, silicon compounds, polymers, metals.	
UNIT II - MEMS FABRICATION TECHNOLOGIES	(9)
Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, and Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wetetching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect- Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials	
UNIT III -MICRO SENSORS	(9)
Photolithography, Ion Implantation, Diffusion, Oxidation, CVD, Sputtering Etching techniques, Micromachining: Bulk Micromachining, Surface Micromachining, LIGA.	
UNIT IV -MICRO ACTUATORS	(9)
Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces, Case Study :RF Switch.	

UNIT V -NANO DEVICES	(9)
Atomic Structures and Quantum Mechanics, Shrodinger Equation, ZnO nano rods based NEMS device: Gas sensor.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. Sergey Edward Lyshevski, “MEMS and NEMS Systems”, Devices, and Structures”,2018 2. Chang Liu, “Foundations of MEMS”, Pearson education India limited, 2006. 3. Marc Madou, “Fundamentals of Microfabrication”, CRC press 1997. 4. Stephen D. Senturia, “Micro system Design”, Kluwer Academic Publishers,2001 5. Sergey Edward Lyshevski, “MEMS and NEMS: Systems, Devices, and Structures” CRCPress, 2002. 6. Tai Ran Hsu ,”MEMS and Microsystems Design and Manufacture” ,Tata Mcraw Hill, 2002.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	2	-	3	1	-	2	2	1
2	2	-	1	2	1	-	3	2
3	3	1	-	3	1	2	2	2
4	2	-	1	2	1	1	2	1
5	-	1	2	1	1	2	2	2
CO (W.A)	2.25	1	1.75	1.8	1	1.75	2.2	1.6

C. N. Ma

22VLX10 NANO SCALE DEVICES					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	Provides knowledge of various industrial applications of Nanotechnology.	1.1	The student will be able to understand the bases for introduction to Nanotechnology.		
2.0	Introduces the theory and practice on Nano materials.	2.1	The student will be able to understand the synthesis of Nano materials and their application and the impact of Nano materials on environment.		
3.0	Imparting the state of art of nanotechnology to the society and to the environmental implication.	3.1	The student will be able to acquire knowledge about various kind of Nano materials.		
4.0	To exercise the students' knowledge and imagination of Nano science and nanotechnology toward engineering applications coupled with detailed justifications.	4.1	The student will be able to understand the Nanotechnology devices used and their structures.		
5.0	It deals with the idea of nano devices.	5.1	The student will be able to understand and improve the application of Nanotechnology.		

UNIT I - NANOTECHNOLOGY	(9)
What is Nanotechnology, types of Nanotechnology and Nano-machines, top down and bottom up techniques, atomic manipulation-Nano dots, semi-conductor quantum dots, self assembly mono layers, simple details of characterization tools- SEM, TEM, STM, AFM.	
UNIT II - NANOMATERIALS	(9)
Background, what is Nanotechnology, types of Nanotechnology and Nano-machines, top down and bottom up techniques, atomic manipulation-Nano dots, semi-conductor quantum dots, self assembly mono layers, simple details Of characterization tools- SEM, TEM, STM, AFM.	
UNIT III - CARBON TUBES	(9)
New forms of carbon, carbon tubes-types of Nano tubes, formation of Nano tubes, assemblies, purification of carbon Nano tubes, properties of Nano tubes, applications of Nano tubes.	

UNIT IV - OPTICS, PHOTONICS AND SOLAR ENERGY	(9)
Light and Nanotechnology, interaction of light and Nanotechnology, Nano holes and photons, solar cells, optically useful Nano structured polymers, photonic crystals.	
UNIT V - FUTURE APPLICATIONS	(9)
MEMS, Nano machines, Nano devices, Quantum Computers, Opto-electronic Devices, Quantum Electronic devices, environmental and biological applications.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. Sergey Edward Lyshevski, "MEMS and NEMS Systems, Devices, and Structures",2018 2. Chang Liu, "Foundations of MEMS", Pearson education India limited, 2006. 3. Marc Madou, "Fundamentals of Microfabrication", CRC press 1997. 4. Stephen D. Senturia," Micro system Design", Kluwer Academic Publishers,2001 5. Sergey Edward Lyshevski, "MEMS and NEMS: Systems, Devices, and Structures" CRCPress, 2002. 6. Tai Ran Hsu ,"MEMS and Microsystems Design and Manufacture" ,Tata Mcraw Hill, 2002.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	2	-	3	1	-	2	2	1
2	2	-	1	2	1	-	3	2
3	3	1	-	3	1	2	2	2
4	2	-	1	2	1	1	2	1
5	-	1	2	1	1	2	2	2
CO (W.A)	2.25	1	1.75	1.8	1	1.75	2.2	1.6

C.N. Ma

22VLX11 NETWORKS ON CHIP					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To Understand the concept of network - on - chip.		1.1	The Students will be able to Compare different architecture design.	
2.0	To Learn router architecture designs.		2.1	The Students will be able to Implement three dimensional networks - on-chip architectures.	
3.0	To study the characteristics of routing algorithms.		3.1	The Students will be able to implement different routing algorithms.	
4.0	To Study fault tolerance network - on-chip.		4.1	The Students will be able to Optimize design in terms of test and fault tolerance of Noc.	
5.0	To learn Three-Dimensional Networks-on-Chips.		5.1	The Students will be able to Optimize Chip Protocols & On-Chip Processor traffic.	

UNIT I - INTRODUCTION TO NOC	(9)
Introduction to NoC – OSI layer rules in NoC - Interconnection Networks in Network-on-Chip Network Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality-of-Service Support.	
UNIT II - ARCHITECTURE DESIGN	(9)
Switching Techniques and Packet Format - Asynchronous FIFO Design -GALS Style of Communication - Wormhole Router Architecture Design - VC Router Architecture Design - Adaptive Router Architecture Design.	
UNIT III - ROUTING ALGORITHM	(9)
Packet routing-Qos, congestion control and flow control – router design – network link design – Efficient and Deadlock-Free Tree-Based Multicast Routing Methods - Path-Based Multicast Routing for 2D and 3D Mesh Networks- Fault-Tolerant Routing Algorithms - Reliable and Adaptive Routing Algorithms.	
UNIT IV - TEST AND FAULT TOLERANCE OF NOC	(9)
Design-Security in Networks-on-Chips-Formal Verification of Communications in Networks-on Chips-Test and Fault Tolerance for Networks-on-Chip Infrastructures-Monitoring Services for Networks-on-Chips.	

UNIT V - THREE-DIMENSIONAL INTEGRATION OF NETWORK-ON-CHIP	(9)
Three-Dimensional Networks-on-Chips Architectures. – A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures - Resource Allocation for QoS On-Chip Communication – Networks-on-Chip Protocols-On-Chip Processor Traffic Modeling for Networks-on-Chip.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<p>1. Wayne Wolf, “Modern VLSI Design – System – on – Chip Design”, Prentice Hall, 3rd Edition, 2008.</p> <p>2. Wayne Wolf , “Modern VLSI Design – IP based Design”, Prentice Hall, 4th Edition, 2008.</p> <p>3. Palesi, Maurizio, Daneshtalab, Masoud “Routing Algorithms in Networks-On-Chip” 2014.</p> <p>4. Konstantinos Tatas and Kostas Siozios "Designing 2D and 3D Network-On-Chip Architectures" 2013.</p>

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	1		2				1	
2	1		2					2
3	1		2					2
4			2		3		2	2
5	1		2		3		1	2
CO (W.A)	1		2		3		1.33	2

C. N. Ma

22VLX12 PHYSICAL DESIGN OF VLSI CIRCUITS					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : 22VLB04 COMPUTER AIDED DESIGN FOR VLSI SYSTEMS					
Course Objectives			Course Outcomes		
1.0	To Learn the basics of Layout Rules.	1.1	The student will be able to know about the basics of Layout Methodologies.		
2.0	To acquire sound knowledge in Top-Down Approach.	2.1	The student will be able to analyze the various characteristics of FPGA.		
3.0	To understand the concept of Performance Issues in Circuit Layout.	3.1	The student will be able to understand the various Power Minimization techniques.		
4.0	To study the concept of Single-Layer Routing and Applications.	4.1	The students will be able to know about the characteristics of Planar Subset Problem.		
5.0	To study the concept of Cell Generation and Programmable Structures.	5.1	The student will be able to apply the CMOS Cell Layout Generation Techniques in various applications.		

UNIT I – VLSI TECHNOLOGY	(9)
Layout Rules and Circuit Abstraction, Cell Generation, Programmable Logic Arrays, Transistor Chaining, Weinberger Arrays and Gate Matrices, Layout Environments, Layout Methodologies, Packaging, Computational Complexity, Algorithmic Paradigms.	
UNIT II - THE TOP-DOWN APPROACH	(9)
Partitioning, Floor planning, Placement, Fundamentals, Maze Running, Line Searching, Steiner Trees, Global Routing, Detailed Routing, Channel Routing, Switchbox Routing, Routing in Field-Programmable Gate Arrays, Array-based FPGAs, Row-based FPGAs.	
UNIT III- PERFORMANCE ISSUES IN CIRCUIT LAYOUT	(9)
Delay Models, Timing-Driven Placement, Timing-Driven Routing, Delay Minimization, Clock Skew Problem, Buffered Clock Trees, Via Minimization, Power Minimization, Discussion and Other Performance Issues, ID Compaction, 2D Compaction.	
UNIT IV - SINGLE-LAYER ROUTING AND APPLICATIONS	(9)
Planar Subset Problem(PSP), Single-Layer Global Routing, Single-Layer Detailed Routing, Wire-Length and Bend Minimization Techniques, Length Minimization, Bend Minimization, Over-the-Cell(OTC)Routing, Physical Model of OTC Routing, Basic Steps in OTC Routing, Multichip Modules (MCMs).	

UNIT V- CELL GENERATION AND PROGRAMMABLE STRUCTURES	(9)
Programmable Logic Arrays, Transistor Chaining, Weinberger Arrays and Gate Matrix Layout, Other CMOS Cell Layout Generation Techniques, CMOS Cell Layout Styles Considering Performance Issues.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. Sarafzadeh, C.K. Wong, “An Introduction to VLSI Physical Design” , Mc Graw Hill International Edition 1995 2. Preas M. Lorenzatti, “Physical Design and Automation of VLSI systems” , The Benjamin Cummins Publishers, 1998. 3. H.Gerez, “Algorithms for VLSI Design Automation”, John Wiley & Sons, 2002 4. N.A Sherwani, “Algorithms for VLSI Physical Design Automation”, Kluwer Academic Publishers, 2002. 5. R .Drechsler, “Evolutionary Algorithms for VLSI CAD”, Boston, Kluwer Academic Publishers, 2010. 6. D.Hill, D.Shugard, J.Fishburn and K.Keutzer, “Algorithms and Techniques for VLSI Layout Synthesis”, Kluwer Academic Publishers, Boston, 1990.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	2	3			3		3	2
2	3	2			2		3	2
3	2			3			3	2
4	2	3				3	3	2
5	3	2	2				3	2
CO (W.A)_	2.4	2.5	2	3	2.5	3	3	2

C.N. Ma

22VLX13 RECONFIGURABLE ARCHITECTURES					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : 22VLX02 ASIC DESIGN					
Course Objectives			Course Outcomes		
1.0	To learn about basics of reconfigurable architecture	1.1	The student will be able to Interpret the concept of reconfigurable systems		
2.0	To present different FPGA technologies & architecture	2.1	The students will be able to understand programmed FPGAs		
3.0	To provide idea about the routing concepts for FPGA	3.1	The students will be able to deal with flexibility and reconfigurability for FPGA		
4.0	To provide knowledge about different high level design style	4.1	The students will be able to deal with different FPGA design styles		
5.0	It deals with the application development with FPGA	5.1	The student will be able to familiarized with the applications development with FPGA		

UNIT I - INTRODUCTION TO RECONFIGURABLE ARCHITECTURES	(9)
Domain-specific processors, Application specific processors, Reconfigurable Computing Systems –Evolution of reconfigurable systems – Characteristics of RCS advantages and issues. Fundamental concepts & Design steps –classification of reconfigurable architecture-fine, coarse grain & hybrid architectures	
UNIT II - FPGA TECHNOLOGIES & ARCHITECTURE	(9)
Technology trends- Programming technology- SRAM programmed FPGAs, antifuse programmed FPGAs, erasable programmable logic devices. Alternative FPGA architectures: Mux Vs LUT based logic blocks – CLB Vs LAB Vs Slices- Fast carry chains- Embedded RAMs- FPGA Vs ASIC design styles.	
UNIT III -ROUTING FOR FPGAS	(9)
General Strategy for routing in FPGAs- routing for row-based FPGAs – segmented channel routing, definitions- Algorithm for I segment and K segment routing – Routing for symmetrical FPGAs, Flexibility of FPGA Routing Architectures: FPGA architectural flexibility on Routability- Effect of switch block flexibility on routability - Tradeoffs in flexibility of S and C blocks	
UNIT IV -HIGH LEVEL DESIGN	(9)
FPGA Design style: Technology independent optimization- technology mapping- Placement. High level synthesis of reconfigurable hardware, high- level languages, Design tools: Simulation (cycle based, event driven based) – Synthesis (logic/HDL vs physically aware) – timing analysis (static vs dynamic)- verification physical design tools.	

UNIT V -APPLICATION DEVELOPMENT WITH FPGAS	(9)
Case Studies of FPGA Applications–System on a Programmable Chip (SoPC) Designs.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. Lev Kirischian, “Reconfigurable Computing Systems Engineering Virtualization of Computing Architecture” 2021 2. Christophe Bobda, “Introduction to Reconfigurable Computing –Architectures, Algorithms and Applications”, Springer, 2010. 3. Clive “Max” Maxfield, “The Design Warrior’s Guide to FPGAs: Devices, Tools And Flows”, Newnes, Elsevier, 2006. 4. Jorgen Staunstrup, Wayne Wif, “Hardware/Software Co- Design: Priciples and practice”, Kluwer Academic Pub, 1997. 5. Maya B. Gokhale and Paul S. Graham, “Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays”, Springer, 2005.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	1
1	2	1	2	-	2	1	2	1
2	2	-	1	1	2	1	2	1
3	1		-	2	1	2	3	2
4	2	-	2	2	2	-	2	1
5	1	2	1	2	1	2	3	2
CO(W.A)	1.6	1.3	1.5	1.75	1.6	1.5	2.4	1.4

C.N. Ma

22VLX14 RFIC DESIGN					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives		Course Outcomes			
1.0	To learn the importance and issues in the design of RF.	1.1	The student will be able to understand the problems created in RF Design.		
2.0	To design the RF filter.	2.1	The student will be able to know about the RF filter design.		
3.0	To learn the concepts of active RF Components and its applications.	3.1	The student will be able to gain knowledge on active RF Components.		
4.0	To know the design for RF amplifier.	4.1	The student will be able to design the RF amplifier circuits.		
5.0	To study about the characteristics of oscillators, mixers, PLL, wireless synthesizers and detector Circuits.	5.1	The student will be able to learn the uses of Oscillators and Mixers in RF designs.		

UNIT I – INTRODUCTION TO RF DESIGN	(9)
Importance of RF design- Electromagnetic spectrum, Introduction to MOSFET physics, RF behavior of passive components, chip Components and circuit board considerations, scattering parameters, smith chart and applications.	
UNIT II - RF FILTER DESIGN	(9)
Overview, Impedance Matching, Basic resonator and filter configuration, special filter realizations, smith chart based filter Design, coupled filter	
UNIT III - ACTIVE RF COMPONENTS AND NETWORKS	(9)
RF diodes, BJT, RF FET'S, High electron mobility transistors, matching and biasing networks impedance matching using discrete components, micro strip line matching networks, amplifier classes of operation and biasing networks.	
UNIT IV - RF AMPLIFIER DESIGN	(9)
Characteristics, amplifier power relations, stability considerations, constant gain circles, constant VSWR circles, low noise circles broadband, high power and multistage amplifier, Noises in receivers and transmitters.	

UNIT V - OSCILLATORS, MIXERS	(9)
Basic oscillator model, High Frequency oscillator configuration, basic characteristic of mixers, wireless synthesizers, phase locked loops, detector and demodulator circuits	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. Reinhold Ludwig and Powel Bretchko, "RF Circuit Design -Theory and Applications", Pearson Education Asia, 1st Edition, 2001. 2. Joseph. J. Carr, "Secrets of RF Circuit Design", McGraw Hill Publishers, 3rd Edition, 2000. 3. Ulrich L. Rohde and David P. New Kirk, "RF / Microwave Circuit Design", John Wiley & Sons USA 2000. 4. Roland E. Best, "Phase - Locked Loops: Design, simulation and applications", McGraw Hill Publishers 5th Edition 2003. 5. B.Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2001.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	1	3	2	2	2	2	3
2	2	1	2	3	2	1	2	2
3	2	1	2	2	2	2	3	2
4	3	1	2	2	2	1	2	2
5	2	2	2	3	2	2	3	2
CO (W.A)	2.4	1.2	2.2	2.4	2	1.6	2.4	2

22VLX15 POWER MANAGEMENT AND CLOCK DISTRIBUTION CIRCUITS					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To design of reference circuits and low dropout regulators for desired specifications	1.1	The students will be able to design band gap reference circuits and low drop out regulator for a given specification.		
2.0	To understand the features of specification related to supply and clock generation circuits of IC	2.1	The students will be able to understand specification related to supply and clock generation circuits of IC		
3.0	To understand oscillators choice and requirements for clock generation circuits	3.1	The students will be able to choose oscillator topology and design meeting the requirement of clock generation circuits.		
4.0	Be exposed to design clock generation and recovery in the context of high-speed systems	4.1	The students will be able to design clock generation circuits in the context of high speed I/Os, high speed broad band communication circuits and data conversion circuits.		
5.0	To understand the various clock distribution circuits.	5.1	The students will be able to Design clock distribution circuits.		

UNIT I - VOLTAGE AND CURRENT REFERENCES	(9)
Current mirrors – self-biased current reference – startup circuits – VBE based current reference – VT based current reference – supply independent biasing – temperature independent biasing.	
UNIT II - LOW DROP OUT REGULATORS	(9)
Analog building blocks – negative feedback – performance metrics – AC design – stability – internal and external compensation – internal and external compensation circuits.	
UNIT III - OSCILLATOR FUNDAMENTALS	(9)
General considerations – ring oscillators – LC oscillators – Colpitts oscillator – jitter and phase noise in ring oscillators – impulse sensitivity function for LC & ring oscillators – phase noise in differential LC oscillators.	
UNIT IV - CLOCK DISTRIBUTION CIRCUITS	(9)
PLL fundamental – PLL stability – noise performance – charge-pump PLL topology – CPPLL building blocks – jitter and Phase noise Performance	

UNIT V -CLOCK AND DATA RECOVERY CIRCUITS	(9)
CDR architectures – trans-impedance amplifiers and limiters – CMOS interface – linear half rate CMOS CDR circuits – wide capture range CDR circuits.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:

1. Gabriel.a. Rincon-Mora, "Voltage References from Diode to Precision Higher Order Band gap circuits", John Wiley & Sons Inc, 2002.
2. Gabriel.a. Rincon-Mora, "Analog IC Design with Low-Dropout Regulators", Mcgraw-Hill Professional Pub, 2009.
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata Mcgraw Hill, 2001.
4. Floyd M. Gardner , "Phase Lock Techniques" ,John Wiley& Sons, Inc 2005.
5. MichielSteyaert, Arthur H.M. Van Roermund, Herman Casier, "Analog Circuit Design: High Speed Clock and Data Recovery, High-Performance Amplifiers Power Management", Springer, 2008.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	2	3	2	2	1	3	1
2	3	1	3	2	1	-	3	-
3	3	-	2	2	-	-	3	-
4	3	-	3	2	2	2	2	-
5	3	1	2	2	2	2	3	2
CO(W.A)	3	1.33	2.6	2	3	1.75	2.8	1.5

C.N.M.

22VLX16 SYSTEM VERILOG					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To Apply System Verilog Concepts to Do Synthesis, Analysis and Architecture Design.	1.1	The student will be able to create correct, efficient, and re-usable models for digital designs using system verilog		
2.0	Understanding of System Verilog and SVA for Verification and Understand The Improvements in Verification Efficiency.	2.1	The student will be able to use system verilog to create test benches for digital designs		
3.0	Understand Advanced Verification Features, Such As The Practical Use of Classes, Randomization, Checking, and Coverage.	3.1	The student will be able to understand and effectively exploit new constructs in System Verilog for verification		
4.0	Knowledge to Communicate The Purpose and Results of a Design Experiment in Written and Oral	4.1	The student will be able to understand the communication between modules		
5.0	Understand The Purpose of Hardware-Software Verification	5.1	The student will be able to designing a complete system model using Verilog		

UNIT I - VERIFICATION METHODOLOGY	(9)
Verification Guidelines: Introduction, Verification Process, Verification Plan, Verification Methodology Manual, Basic Test bench Functionality, Directed Testing, Methodology Basics, Constrained-Random Stimulus, Functional Coverage, Test bench Components, Layered Test bench	
UNIT II - SYSTEM VERILOG BASICS AND CONCEPTS	(9)
Data Types: Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Creating New Types With Type def, Creating User-Defined Structures, Enumerated Types, Constants, Strings. Procedural Statements and Routines: Procedural Statements, Tasks, Functions, and Void Functions	
UNIT III - OOPS	(9)
Introduction-Where to Define a Class- OOPS Terminology -Creating New Objects –Object Deallocation-Using Objects -Static Variables Vs. Global Variables -Class Routines –Defining Routines Outside of The Class - Scoping Rules -Using One Class Inside Another - Understanding Dynamic Objects -Copying Objects - Public Vs. Private -Straying Off Course - Building a Test bench	

UNIT IV - THREADS AND INTER-PROCESS COMMUNICATION AND FUNCTIONAL COVERAGE	(9)
Working With Threads, Inter-Process Communication, Events, Semaphores, Mailboxes, Building a Test bench With Threads and IPC. Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Coverage Options, Parameterized Cover Groups, Analysing Coverage Data, Measuring Coverage Statistics	
UNIT V - COMPLETE DESIGN MODEL USING SYSTEM VERILOG- CASE STUDY	(9)
System Verilog ATM Example, Data Abstraction, Interface Encapsulation, Design Top Level Squat, Receivers and Transmitters, Test Bench for ATM.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:

1. Chris Spear, "System Verilog for Verification: a Guide to Learning the Test bench Language Features" , Springer 2006.
2. Janick Bergeron, Kluwer , "Writing Test benches: Functional Verification of HDL Models", 2nd Edition, Academic Publishers, 2003.
3. Stuart Sutherland, Simon David man and Peter Flake, "System Verilog for Design: a Guide to Using System Verilog for Hardware Design and Modelling", 2nd Edition, Springer
4. "Mark Glasser, Open Verification Methodology Cookbook, Springer, 2009
5. Harry D. Foster, Adam C. Krolnik, David J. Lacey, Kluwer "Assertion-Based Design, 2nd Edition, Academic Publishers, 2004.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	-	3	-	3	3	3	3
2	1	-	2	-	3	2	3	3
3	3	-	3	-	3	3	2	3
4	3	-	3	-	2	3	3	2
5	2	-	3	-	2	3	2	3
CO(W.A)	1.8	-	2.8	-	2.6	2.8	2.6	2.8

C. N. Ma...

22VLX17 SYSTEM ON CHIP					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To Learn the basics of SoC.	1.1	The student will be able to identify, formulate and treat complex issues in the field of system-on-chip from a holistic perspective.		
2.0	To acquire sound knowledge in design methodology.	2.1	The student will be able to analyze the performance of SoC based design by various advanced techniques.		
3.0	To understand the different types of memory design.	3.1	The student will be able to apply System C for system design.		
4.0	To study the concept of IP based system design.	4.1	The students will be able to know about the characteristics of Non-quasi-static Modeling.		
5.0	To study the concept of Soft Processors and Hard Processors.	5.1	The student will be able to apply the static timing analysis for a SoC based design.		

UNIT I - SOC INTRODUCTION	(9)
Components of SOC- Design flow – Nature of Hardware & Software, driving factors for hardware- software co design -design space, system specification and modeling – Hardware software trade offs-Co-design approaches- Models of Computation	
UNIT II - DESIGN METHODOLOGY FOR LOGIC, MEMORY AND ANALOG CORES	(9)
Guidelines for design reuse - Efficiency of application specific hardware - Target architectures for HW/SW partitioning -System Integration, Embedded memories – design methodology for embedded memories – Specification of analog cores	
UNIT III - MEMORY DESIGN	(9)
SoC external memory, SoC internal memory, Scratch pads and cache memory – cache organization and write policies– multilevel caches – SoC memory systems – board based memory systems – simple processor / memory interaction.	

UNIT IV - IP BASED SYSTEM /DESIGN	(9)
Types of IP, IP across design hierarchy-IP life cycle- Creating and using IP-Technical concerns on IP reuse-Integration – IP evaluation on FPGA prototypes	
UNIT V - FPGA BASED EMBEDDED PROCESSOR	(9)
Hardware software task partitioning – FPGA fabric Immersed Processors – Soft Processors and Hard Processors – Tool flow for Hardware/Software Co-design - Types of On-chip interfaces – Wishbone interface, Avalon Switch, FPGA-based Signal Interfacing and Conditioning.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> Wayne Wolf, “Modern VLSI Design – System – on – Chip Design”, Prentice Hall, 3rd Edition, 2008. Wayne Wolf , “Modern VLSI Design – IP based Design”, Prentice Hall, 4th Edition, 2008. Jose L. Ayala, “Communication Architectures for Systems-on-Chip”, CRC Press, 1st Edition, 2011. Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, “System-on-Chip Test Architectures: Nanometer Design for Testability”, 1st Edition, 2010. Rochit Rajsuman, “System-on- a-chip: Design and test”, Advantest America R & D Center, 2000

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	2	-	3	3	-	3	2
2	3	2	2	2	3	-	3	1
3	-	1	2	-	1	2	2	2
4	3	3	2	2	3	2	3	2
5	3	3	-	1	2	-	3	2
CO (W.A)	3	2.5	2	2	2.75	2	2.8	1.8

C.N.M.

22VLX18 VLSI FOR IOT SYSTEMS					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives		Course Outcomes			
1.0	To Learn the introduction of IoT.	1.1	The student will be able to infer the components of IOT and integrate it to integrated circuits to design an electronic system.		
2.0	To acquire sound knowledge in Types of sensors used in IoT.	2.1	The student will be able to analyze the performance of SoC based design by various advanced techniques.		
3.0	To understand the concept of Application Processors.	3.1	The student will be able to apply System C for system design		
4.0	To study the concept of FPGA.	4.1	The students will be able to know about the characteristics of Non-quasi-static Modeling.		
5.0	To study the applications of IoT.	5.1	The student will be able to apply the static timing analysis for a SoC based design		

UNIT I – INTRODUCTION of IoT	(9)
Concept of connected world - Need, Legacy systems for connected world-features and limitations, Key features of IoT architecture, Merits and Demerits of IoT technology. Applications driven by IoT technology	
UNIT II - COMPONENTS OF IoT	(9)
Basic building blocks of an IoT system - Artificial Intelligence, Connectivity. Sensors and Computing nodes. Sensors used in IoT systems characteristics and requirements. Types of sensors properties for IoT systems – compute nodes of IoT, Connectivity technologies in IoT	
UNIT III - IC TECHNOLOGY FOR IoT	(9)
SoC architecture for IoT Devices - Application Processors, Microcontrollers, Smart Analog, Memory architecture for IoT - Non Volatile Memories (NVM). Embedded Non-Volatile Memories – Low Dropout Regulator, DC-to-DC Converters, Voltage References, Power Management Units (PMUS) in IC's and Systems, Role of Field Programmability in IoT systems.	
UNIT IV - ELECTRONIC SYSTEM DESIGN FOR IoT	(9)
Electronic System Design for IoT - Requirements, Computing blocks in IoT systems - MCU's, DSPS and FPGA, System Power Supply Design for IoT systems, Component models & System Design - System Level Integration, Operating conditions of IoT devices and impact on Electronic System Design, Hardware Security issues, EMI/EMC, SI/PI and Reliability Analysis in IOT systems.	

UNIT V - APPLICATIONS of IoT	(9)
Automated Design of Reconfigurable Micro architectures for Accelerators Under Wide-Voltage Scaling - Approximate Adder Circuits Using Clocked CMOS Adiabatic Logic (CCAL) for IoT Applications -Battery Management Technique to Reduce Standby Energy Consumption in Ultra-Low Power IoT and Sensory Applications.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> Alloto. "Enabling the Internet of Things- From Integrated Circuits to Integrated Systems", Springer Publications, 1st Edition, 2017. Pieter Harpe, Kofi A. A Makinwa, Andrea Baschirotto, "Hybrid ADCs, Smart Sensors for the IoT, and Sub-IV & Advanced Node Analog Circuit Design". Springer International Publishing AG, 2017. Rashid Khan, Kajari Ghosh dastidar, AjithVasudevan, "Learning IoT with Particle Photon and Electron". Packt Publishing Limited (Verlag), 2016. Apekmulay, "Sustaining Moore's Law : Uncertainty Leading to a Certainty of IoT Revolution", Morgan and Claypool Publishers, 2015. Jim Lipman sidense Corp, "NVM Memory : A Critical Design consideration for IoT Applications"- https://www.design-reuse.com/articles/32614/nvm-memory-iot-applications.html

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	2	2	3	3	-	3	2
2	3	2	1	2	3	-	3	1
3	2		2		1	1	2	2
4	2	3	2	2	3	2	3	2
5	3	2	-	1	2	-	3	2
CO(W.A)	2.6	2.3	1.8	2.0	2.4	1.5	2.8	1.8

C.N. Mani

22VLX19 SOFT COMPUTING AND OPTIMIZATION TECHNIQUES					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To learn the key aspects of soft computing and Neural networks.	1.1	The students will be able to analysis and Design of Synchronous and Asynchronous sequential machines		
2.0	To understand the features of neural network and its applications.	2.1	The students will be able to draw a ASM chart for digital designs		
3.0	To expose the key aspects of Fuzzy Logic systems.	3.1	The students will be able to detect and diagnosis different faults in digital circuits		
4.0	Be exposed to neuro-fuzzy hybrid systems and its applications.	4.1	The students will be able to Model Neuro Fuzzy system for clustering and classification.		
5.0	To understand the various evolutionary optimization techniques.	5.1	The students will be able to use the optimization techniques to solve the real-world problems.		

UNIT I - INTRODUCTION TO SOFT COMPUTING	(9)
Evolution of Computing – Soft Computing Constituents – From Conventional AI to Computational Intelligence-Machine Learning Basics.	
UNIT II - NEURAL NETWORKS	(9)
Machine Learning using Neural Network, Adaptive Networks – Feed Forward Networks–Supervised Learning Neural Networks – Reinforcement Learning –Unsupervised Learning Neural Networks – Adaptive Resonance Architectures.	
UNIT III - FUZZY LOGIC	(9)
Fuzzy Sets – Operations on Fuzzy Sets – Fuzzy Relations– Membership Functions-Fuzzy Rules and Fuzzy Reasoning– Fuzzy Inference Systems – Fuzzy Expert Systems – Fuzzy Decision Making.	
UNIT IV - NEURO-FUZZY MODELING	(9)
Adaptive Neuro – Fuzzy Inference Systems – Coactive Neuro – Fuzzy Modeling –Classification and Regression Trees – Data Clustering Algorithms – Rule base Structure Identification – Neuro – Fuzzy Control.	

UNIT V -CONVENTIONAL OPTIMIZATION TECHNIQUES	(9)
Introduction to optimization techniques – classification – Unconstrained optimization-gradient search method – Newton’s Method, Marquardt Method, Constrained optimization – Interior penalty function method – external penalty function method.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. Jyh-Shing RogerJang, Chuen-TsaiSun, EijiMizutani, “Neuro-Fuzzy and Soft Computing”, Prentice-Hall of India,2003. 2. David E. Goldberg, Genetic Algorithms in Search, Optimization and Machine Learning, Addison wesley, 2009. 3. Kwang H.Lee, “First course on Fuzzy Theory and Applications”, Springer–Verlag Berlin Heidelberg, 2005. 3. Georgej Klirandboyuan, “fuzzy sets and fuzzy logic – theory and applications”, prentice-hall, 1995. 4. James a. freeman and David M.skapura, “Neural networks algorithms, applications, and programming techniques”, pearson edn.,2003..

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	2	2	3	3	1	3	2
2	3	1	2	2	3	-	3	2
3	2	-	2	2	-	1	3	3
4	3	3	2	2	3	2	2	2
5	3	3	1	2	3	2	3	2
CO (W.A)	2.8	2.25	1.8	2.75	3	1.5	2.8	2.2

C.N.M.

22VLX20 HARDWARE AND SOFTWARE CO-DESIGN FOR FPGA					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To study and compare the co-design approaches for single processor and multiprocessor architectures.	1.1	The student will be able to describe The Broad Range of System Architectures and Design Methodologies that currently exist and define their fundamental attributes.		
2.0	To know the various techniques of Hardware and software partitioning.	2.1	The student will be able to discuss the Dataflow Models as a State-of-the-Art Methodology to Solve Co-Design Problems and to Optimize the balance between Software and Hardware.		
3.0	To acquire the knowledge about hardware and software co-synthesis.	3.1	The student will be able to understand in Translating between Software and Hardware Descriptions through Co-Design Methodologies.		
4.0	To study the various proto type techniques and architectures.	4.1	The student will be able to understand the State-of-The-Art practices in developing Co-Design Solutions to problems using modern Hardware/Software Tools for building prototypes.		
5.0	To learn and implement the design specific language.	5.1	The student will be able to understand the Concurrent Specification from an Algorithm, Analyze its behavior and partition the Specification into Software (C Code) and Hardware (HDL) Components		

UNIT I - SYSTEM SPECIFICATION AND MODELLING	(9)
Embedded Systems, Hardware/Software Co-Design, Co - Design for System Specification and Modeling, Co – Design for Heterogeneous Implementation - Processor Synthesis, Single – Processor Architectures with one ASIC, Single Processor Architectures with many ASICs Processor Architectures, Comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification	
UNIT II - HARDWARE/SOFTWARE PARTITIONING	(9)
The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph , Formulation of the HW/SW Partitioning Problem , Optimization , HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.	
UNIT III - HARDWARE/SOFTWARE CO-SYNTHESIS	(9)
The Co - Synthesis Problem, State - Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis	

UNIT IV - PROTOTYPING AND EMULATION	(9)
Introduction, Prototyping and Emulation Techniques , Prototyping and Emulation Environments ,Future Developments in Emulation and Prototyping, Target Architecture Specialization Techniques ,System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems ,Mixed Systems and Less Specialized Systems	
UNIT V - DESIGN SPECIFICATION AND VERIFICATION	(9)
Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System Level Specification and Design System - Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-simulation	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. Ralf Niemann, "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Pub, 1998. 2. Jorgen Staunstrup, Wayne Wolf , "Hardware/Software Co-Design: Principles and Practice" , Kluwer Academic Pub, 1997. 3. Giovanni De Micheli, Rolf Ernst Morgon, " Reading in Hardware/Software Co-Design" Kaufmann Publishers, 2001.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	-	3	-	3	3	3	3
2	1	-	2	-	3	2	3	3
3	3	-	3	-	3	3	2	3
4	3	-	3	-	2	3	3	2
5	2	-	3	-	2	3	2	3
CO (W.A)	1.8	-	2.8	-	2.6	2.8	2.6	2.8

C. N. Ma

22VLX2I VLSI FOR WIRELESS COMMUNICATION					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives		Course Outcomes			
1.0	To make students to learn and design low noise amplifiers.	1.1	The student will be able to design components using low noise amplifiers.		
2.0	To enable the student to understand various types of mixers.	2.1	The Students will be able to analyze characteristics of mixers for various operations.		
3.0	To enable the student to understand the concept of PLL and Oscillators.	3.1	The Students will be able to design concept of PLL and various Oscillators.		
4.0	To make the students to analyze data convertors and equalizers.	4.1	The students will be able to analyze the operation data convertors and equalizers.		
5.0	To motivate the students to implement the project using VLSI architecture for Multitier Wireless System.	5.1	The student will be able to implement the project using VLSI architecture for Multitier Wireless System.		

UNIT I - COMPONENTS AND DEVICES	(9)
Integrated inductors, resistors, MOSFET and BJT AMPLIFIER DESIGN: Low Noise Amplifier Design - Wideband LNA - Design Narrowband LNA - Impedance Matching - Automatic Gain Control Amplifiers – Power Amplifiers.	
UNIT II - MIXERS	(9)
Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion - Low Frequency Case: Analysis of Gilbert Mixer – Distortion - High-Frequency Case – Noise - A Complete Active Mixer. Switching Mixer - Distortion in Unbalanced Switching Mixer - Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer -Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer -Extrinsic Noise in Single Ended Sampling Mixer.	
UNIT III - FREQUENCY SYNTHESIZERS	(9)
Phase Locked Loops - Voltage Controlled Oscillators - Phase Detector – Analog Phase Detectors – Digital Phase Detectors - Frequency Dividers - LC Oscillators - Ring Oscillators - Phase Noise - A Complete Synthesizer Design Example (DECT Application).	

UNIT IV - UB SYSTEMS	(9)
Data converters in communications, adaptive Filters, equalizers and transceivers.	
UNIT V - IMPLEMENTATIONS	(9)
VLSI architecture for Multitier Wireless System - Hardware Design Issues for a Next generation CDMA System.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. Bosco H Leung “VLSI for Wireless Communication”, Pearson Education, 2002. 2. B.Razavi ,”RF Microelectronics” , Prentice-Hall ,1998. 3. homas H.Lee, “The Design of CMOS Radio –Frequency Integrated Circuits”, Cambridge University Press, 2003. 4. Emad N Farag and Mohamed I Elmasry, “Mixed Signal VLSI Wireless Design -Circuits and Systems”, Kluwer Academic Publishers, 2000. 5. Behzad Razavi, “Design of Analog CMOS Integrated Circuits” McGraw-Hill, 1999. 6. J. Crols and M. Steyaert, “CMOS Wireless Transceiver Design,” Boston, Kluwer Academic Pub., 1997.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1			2			1	1	2
2				2		2	2	
3				2			2	2
4			2	2			1	1
5	1			2	1		2	3
CO (W.A)	1		2	2	1	1.5	1.6	2

C. N. Ma

22VLX22 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To know about analysis and Design of Transmission line and propagation of signal and design of PCB layer.	1.1	The students will be able to analysis of Transmission line and Design of PCB layer.		
2.0	To learn about Multi-conductor transmission and cross-talk lines.	2.1	The students will be able to conduct and detect the Multi-conductor transmission and cross-talk lines.		
3.0	To learn about different Non-ideal signal return paths and Transmission line losses models.	3.1	The students will be able to detect Non-ideal signal return paths and diagnosis different faults in Transmission line losses models.		
4.0	To Know about Types of Power Considerations and transmission systems design.	4.1	The students will be able to have knowledge of Power Considerations and transmission systems design.		
5.0	To have knowledge about clock distribution and clock oscillators.	5.1	The students will be able to design the clock distribution through clock oscillators.		

UNIT I - SIGNAL PROPAGATION ON TRANSMISSION LINES	(9)
Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance, wave propagation, reflection, and bounce diagrams Reactive terminations – L, C, static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stack ups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for micro strip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion	
UNIT II -MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK	(9)
Multi-conductor transmission-lines, coupling physics, per unit length parameters, Near and far-end cross-talk, minimizing cross-talk (stripline and micro strip) Differential signaling, termination, balanced circuits, S-parameters, Lossy and Lossless models	
UNIT III-NON-IDEAL EFFECTS	(9)
Non-ideal signal return paths – gaps, BGA fields, via transitions, Parasitic inductance and capacitance, Transmission line losses – Rs, tanδ, routing parasitic, Common-mode current, differential-mode current, Connectors	

UNIT IV - POWER CONSIDERATIONS AND SYSTEM DESIGN	(9)
SSN/SSO, DC power bus design, layer stack up, SMT decoupling, Logic families, power consumption, and system power delivery, Logic families and speed Package types and parasitic, SPICE, IBIS models, Bit streams, PRBS and filtering functions of link-path components, Eye diagrams, jitter, inter-symbol interference Bit-error rate, Timing analysis	
UNIT V-CLOCK DISTRIBUTION AND CLOCK OSCILLATORS	(9)
Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, cancelling parasitic capacitance, Clock jitter	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. Douglas Brooks, "Signal Integrity Issues and Printed Circuit Board Design", Prentice Hall PTR, 2003 . 2. Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR, 2003. 3. H. W. Johnson and M. Graham, "High-Speed Digital Design: A Handbook of Black Magic", Prentice Hall, 1993. 4. S. Hall, G. Hall, and J. McCall, "High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices", Wiley-Inter science, 2000

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	2	2	-	2	3	3	2	1
2	2	1	1	1	2	1	3	2
3	3	2	2	1	1	1	-	2
4	1	-	1	2	2	-	2	3
5	3	1	3	3	1	1	1	1
CO (W.A)	2.2	1.2	1.4	1.8	1.8	1.4	1.6	1.8

C.N.Ma

22VLX23 DIGITAL IMAGE AND VIDEO PROCESSING					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives		Course Outcomes			
1.0	To know about digital image fundamentals, image enhancements and filtering	1.1	The students will be able to understand basic of digital image fundamentals, image enhancements and filtering		
2.0	To know about color image processing and segmentation	2.1	The students will be able to know about colour image processing and segmentation		
3.0	To learn about wavelets and multi-resolution image processing	3.1	The students will be to able learn about wavelets and multi-resolution image processing		
4.0	To do and know image compression techniques for different images	4.1	The students will be able do and know image compression techniques for different images		
5.0	To have knowledge about video coding segmentation	5.1	The student will be able to acquire knowledge about video coding segmentation		

UNIT I - DIGITAL IMAGE FUNDAMENTALS	(9)
Elements of visual perception, image sensing and acquisition, image sampling and quantization, basic relationships between pixels – neighborhood, adjacency, connectivity, distance measures. Gray level transformations, histogram equalization and specifications, pixel-domain smoothing filters – linear and order-statistics, pixel domain sharpening filters, frequency domain filters	
UNIT II - COLOUR IMAGE PROCESSING AND SEGMENTATION	(9)
Color models–RGB, YUV, HSI; Color transformations–formulation, color complements, color slicing, tone and color corrections; Color image smoothing and sharpening; Color Segmentation. Detection of discontinuities, edge linking and boundary detection, thresholding: global and adaptive, region-based segmentation.	
UNIT III - WAVELETS AND MULTI-RESOLUTION IMAGE PROCESSING	(9)
Uncertainty principles of Fourier Transform, Time-frequency localization, continuous wavelet transforms, wavelet bases and multi-resolution analysis, wavelets and Sub-band filter banks, wavelet packets.	
UNIT IV - IMAGE COMPRESSION	(9)
Redundancy–inter-pixel and psycho-visual; Lossless compression – predictive, entropy; Lossy compression-predictive and transform coding; Discrete Cosine Transform; Still image compression standards – JPEG and JPEG-2000.	

UNIT V - VIDEO CODING SEGMENTATION	(9)
Inter-frame redundancy, motion estimation techniques – full search, fast search strategies, forward and backward motion prediction, frame classification – I, P and B; Video sequence hierarchy – Group of pictures, frames, slices, macro-blocks and blocks; Elements of a video encoder and decoder; Video coding standards – MPEG and H.26X. Temporal segmentation–shot boundary detection, hard-cuts and soft-cuts; spatial segmentation – motion-based; Video object detection and tracking.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. M. Tekalp ,”Digital video Processing”, Prentice Hall International. 2. Gonzaleze and Woods ,”Digital Image Processing “, 3rd edition , Pearson 3. Yao wang, Joem Ostarmann and Ya – quin Zhang, ”Video processing and communication “,1st edition , PHI.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	2	2	-	1	1	1	2	-
2	2	2	1	1	1	1	-	3
3	2	2	-	1	-	1	-	3
4	2	2	1	-	-	2	1	2
5	2	2	-	-	-	2	1	2
CO (W.A)	2	2	0.4	0.6	0.2	1.4	0.8	2

C. N. Ma

22BAZ01 RESEARCH METHODOLOGY AND IPR					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To understand the basic concepts of research and its methodologies, investigation of solutions for research problem, data collection, analysis and interpretation.	1.1	The student will be able to demonstrate the concepts of research and its methodologies, approaches of information investigation of solutions for research problem, data collection, analysis and interpretation.		
2.0	To identify the various procedures to collect literature studies approaches analysis, plagiarism, and research ethics.	2.1	The student will be able to formulate effective literature studies approaches, analysis, plagiarism, and research ethics.		
3.0	To inculcate knowledge on Effective technical writing and method to write report.	3.1	The student will be able to identify the design for Effective technical writing and how to write report.		
4.0	To provide knowledge process like drawing and drafting tools and reviewing research papers.	4.1	The student will be able to choose the process like drawing and drafting tools and reviewing research papers.		
5.0	To summarize the design for Intellectual property rights and code of ethics.	5.1	The student will be able to formulate the design for Intellectual property rights and code of ethics.		

UNIT I RESEARCH PROBLEM FORMULATION	(9)
Meaning of research problem- Sources of research problem, criteria characteristics of a good research problem, errors in selecting a research problem, scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, necessary instrumentations	
UNIT II LITERATURE REVIEW	(9)
Effective literature studies approaches, analysis, plagiarism, and research ethics	
UNIT III TECHNICAL WRITING /PRESENTATION	(9)
Effective technical writing, how to write report, paper, developing a research proposal, format of research proposal, a presentation and assessment by a review committee.	

UNIT IV INTRODUCTION TO INTELLECTUAL PROPERTY RIGHTS (IPR)	(9)
Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.	
UNIT V INTELLECTUAL PROPERTY RIGHTS (IPR)	(9)
Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System, IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. Cooper, D. R. and Schindler, P. S., (2009), "Business Research Methods", Tata McGraw Hill, 9th Edition. 2. Krishnaswamy, K.N., Sivakumar, A.I., and Mathirajan, M., "Management Research Methodology", Pearson Education , 2006. 3. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd, 2007.

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	2	1	1	2	1	3	
2	2	3	2	1			2	1
3	2	3	2	2	1	1	2	1
4	1	3	2	2	2	1	1	2
5	1	1	2	3	2	2	1	2
CO (W.A)	1.80	2.4	1.80	1.80	1.75	1.25	1.80	1.50

C.N. Ma

22CPZ01 MACHINE VISION					
		L	T	P	C
		3	0	0	3
PRE REQUISITE : NIL					
Course Objectives		Course Outcomes			
1.0	To know the basics of machine vision and computer vision	1.1	The student will be able to apply the vision concepts in various mechatronics applications		
2.0	To study the image acquisition techniques	2.1	The student will be able to recognize the Image acquisition techniques and tools		
3.0	To learn the image processing methods	3.1	The student will be able to apply the image processing tools and libraries		
4.0	To understand the methods used for image analysis	4.1	The student will be able to analyze the images in the case of Robotic or IoT applications		
5.0	To gain exposure on Image processing applications	5.1	The student will be able to select the right machine vision system for implementing in industrial applications		

UNIT I INTRODUCTION	(8)
Human vision – Machine vision and Computer vision – Benefits of machine vision – Block diagram and function of machine vision system implementation of industrial machine vision system – Physics of Light – Interactions of light – Refraction at a spherical surface	
UNIT II IMAGE ACQUISITION	(12)
Scene constraints – Lighting parameters – Lighting sources, Selection – Lighting Techniques – Types and Selection – Machine Vision Lenses and Optical Filters, Specifications and Selection Imaging Sensors – CCD and CMOS, Specifications – Interface Architectures – Analog and Digital Cameras – Digital Camera Interfaces – Camera Computer Interfaces, Specifications and election – Geometrical Image formation models – Camera Calibration	
UNIT III IMAGE PROCESSING	(10)
Machine Vision Software – Fundamentals of Digital Image – Image Acquisition Modes – Image Processing in Spatial and Frequency Domain – Point Operation, Thresholding, Grayscale Stretching – Neighborhood Operations, Image Smoothing and Sharpening – Edge Detection –Binary Morphology – Color image processing.	

UNIT IV IMAGE ANALYSIS	(6)
Feature extraction – Region Features, Shape and Size features – Texture Analysis – Template Matching and Classification – 3D Machine Vision Techniques – Decision Making.	
UNIT V MACHINE VISION APPLICATIONS	(9)
Machine vision applications in manufacturing, electronics, printing, pharmaceutical, textile, applications in non-visible spectrum, metrology and gauging, OCR and OCV, vision guided robotics – Field and Service Applications – Agricultural, and Bio medical field, augmented reality, surveillance, bio-metrics.	
TOTAL (L:45) :45 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. D. A. Forsyth and J. Ponce, “Computer Vision: A Modern Approach”, Pearson Education, 2003. 2. R. Jain, R. Kasturi and B. G. Schunck, “Machine Vision”, McGraw-Hill, 1995. 3. Dana H. Ballard & Christopher M. Brown, “Computer Vision”, Prentice-Hall, 1982. 4. Alexander Hornberg, “Handbook of Machine Vision”, 1st Edition. 5. Emanuele Trucco, Alessandro Verri, “Introductory Techniques For 3D Computer Vision”, 1st Edition

Mapping of COs with POs / PSOs								
COs	POs						PSOs	
	1	2	3	4	5	6	1	2
1	3	2	-	1	1	3	2	2
2	3	2	2	1	1	3	2	2
3	3	2	3	2	1	3	2	3
4	3	2	2	1	1	3	2	2
5	3	3	3	3	3	3	3	3
CO (W.A)	3.00	2.20	2.50	1.60	1.40	3.00	2.20	2.40

C.N.M.

22PGA01 ENGLISH FOR RESEARCH PAPER WRITING					
		L	T	P	C
		2	0	0	0
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To make the students to improve writing skills and level of readability	1.1	The students will be able to improve writing skills and level of readability		
2.0	To explain the strategic planning process and apply different presentation method	2.1	The students will be able to describe what to write in each section		
3.0	To foster the ability to understand and to utilize the mechanics of writing	3.1	The students will be able to explain the skills needed for writing quality research paper		
4.0	To Infer the skills needed when writing the Conclusion	4.1	The students will be able to explore the recent areas of research		
5.0	To focus research and its key variables, guiding through research process	5.1	The students will be able to illustrate the good quality of paper at very first-time submission		

UNIT I - INTRODUCTION	(6)
Planning and Preparation - Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness	
UNIT II - PRESENTATION SKILLS	(6)
Clarifying Who Did What- Highlighting Findings - Hedging and Criticizing- Paraphrasing - Sections of a Paper – Abstracts - Introduction	
UNIT III- MECHANICS OF RESEARCH	(6)
Key skills needed for writing - Title, Abstract, Introduction, Discussion, Conclusion, The Final Check	
UNIT IV - PROCESS OF RESEARCH WRITING	(6)
Skills needed for writing Methods - skills needed when writing Results - skills needed when writing Discussion - skills needed when writing Conclusion.	
UNIT V- QUALITY RESEARCH PAPER	(6)
Useful phrases, Checking Plagiarism - Bibliography- Citation- how to ensure paper is as good as it could possibly be the first- time submission	
TOTAL (L:30) :30 PERIODS	

REFERENCES:

1. Adrian Wallwork , “English for Writing Research Papers”, Springer New York Dordrecht Heidelberg London, 2011
2. Day R., “ How to Write and Publish a Scientific Paper”, Cambridge University Press 2006
3. Goldbort R., “ Writing for Science”, Yale University Press (available on Google Books) 2006
4. Highman N., “ Handbook of Writing for the Mathematical Sciences”, SIAM. Highman’s book 1998.

C. N. Ma

22PGA02 DISASTER MANAGEMENT					
		L	T	P	C
		2	0	0	0
PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To Summarize basics of disaster		1.1	The student will be able to to summarize basics of disaster	
2.0	To Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response		2.1	The student will be able to explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.	
3.0	To Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.		3.1	The student will be able to illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.	
4.0	To Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.		4.1	The student will be able to describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations	
5.0	To Develop the strengths and weaknesses of disaster management approaches		5.1	The student will be able to develop the strengths and weaknesses of disaster management approaches	

UNIT I - INTRODUCTION	(6)
Disaster: Definition, Factors and Significance; Difference between Hazard And Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.	
UNIT II - REPERCUSSIONS OF DISASTERS AND HAZARDS	(6)
Economic Damage, Loss of Human and Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.	
UNIT III- DISASTER PRONE AREAS IN INDIA	(6)
Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides And Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference To Tsunami; Post-Disaster Diseases and Epidemics.	

UNIT IV - DISASTER PREPAREDNESS AND MANAGEMENT	(6)
Preparedness: Monitoring Of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological And Other Agencies, Media Reports: Governmental and Community Preparedness.	
UNIT V- RISK ASSESSMENT	(6)
Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival	
TOTAL (L:30) :30 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. Goel S. L., "Disaster Administration And Management Text And Case Studies", Deep & Deep Publication Pvt. Ltd., New Delhi, 2009. 2. Nishitha Rai, Singh AK, "Disaster Management in India: Perspectives, issues and strategies", New Royal book Company, 2007. 3. Sahni, PardeepEt.Al. ," Disaster Mitigation Experiences and Reflections", Prentice Hall Of India, New Delhi, 2001.

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22PGA03 CONSTITUTION OF INDIA					
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PRE REQUISITE : NIL					
Course Objectives			Course Outcomes		
1.0	To understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.	1.1	The student will be able to discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.		
2.0	To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional	2.1	The student will be able to discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.		
3.0	To role and entitlement to civil and economic rights as well as the emergence nation hood in the early years of Indian nationalism.	3.1	The student will be able to discuss the circumstances surrounding the foundation of the Congress Socialist Party[CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution..		
4.0	To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.	4.1	The student will be able to discuss the passage of the Hindu Code Bill of 1956.		
1.0	To understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.	1.1	The student will be able to discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.		

UNIT I - HISTORY OF MAKING OF THE INDIAN CONSTITUTION	(6)
History, Drafting Committee, (Composition & Working)	
UNIT II - PHILOSOPHY OF THE INDIAN CONSTITUTION	(6)
Preamble, Salient Features	
UNIT III- ONTOURS OF CONSTITUTIONAL RIGHTS AND DUTIES	(6)
Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.	

UNIT IV - LOCAL ADMINISTRATION	(6)
District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO, Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.	
UNIT V- ELECTION COMMISSION	(6)
Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners - Institute and Bodies for the welfare of SC/ST/OBC and women.	
TOTAL (L:30) :30 PERIODS	

REFERENCES:
<ol style="list-style-type: none"> 1. "The Constitution of India", 1950(Bare Act), Government Publication. 2. Dr.S.N.Busi, Dr.B. R., "Ambedkar framing of Indian Constitution", 1st Edition, 2015. 3. M.P. Jain, " Indian Constitution Law", 7th Edition., Lexis Nexis,2014. 4. D.D. Basu, "Introduction to the Constitution of India" , Lexis Nexis, 2015.

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